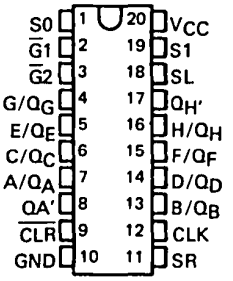
TYPES SN54LS323, SN74LS323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

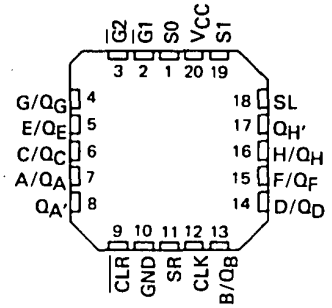
OCTOBER 1976—REVISED APRIL 1985

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
  Hold (Store) Shift Left
  Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Typical Power Dissipation . . . 175 mW
- Guaranteed Shift (Clock) Frequency . . . 25 MHz
- Applications:
  Stacked or Push-Down Registers,
  Buffer Storage, and
  Accumulator Registers
- SN54LS299 and SN74LS299 Are Similar But Have Direct Overriding Clear

SN54LS323 . . . J PACKAGE
SN74LS323 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS323 . . . FK PACKAGE
SN74LS323 . . . FN PACKAGE
(TOP VIEW)



description

These Low-Power Schottky eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table. Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low level at the clear input clears the register on the next low-to-high transition of the clock.

FUNCTION TABLE

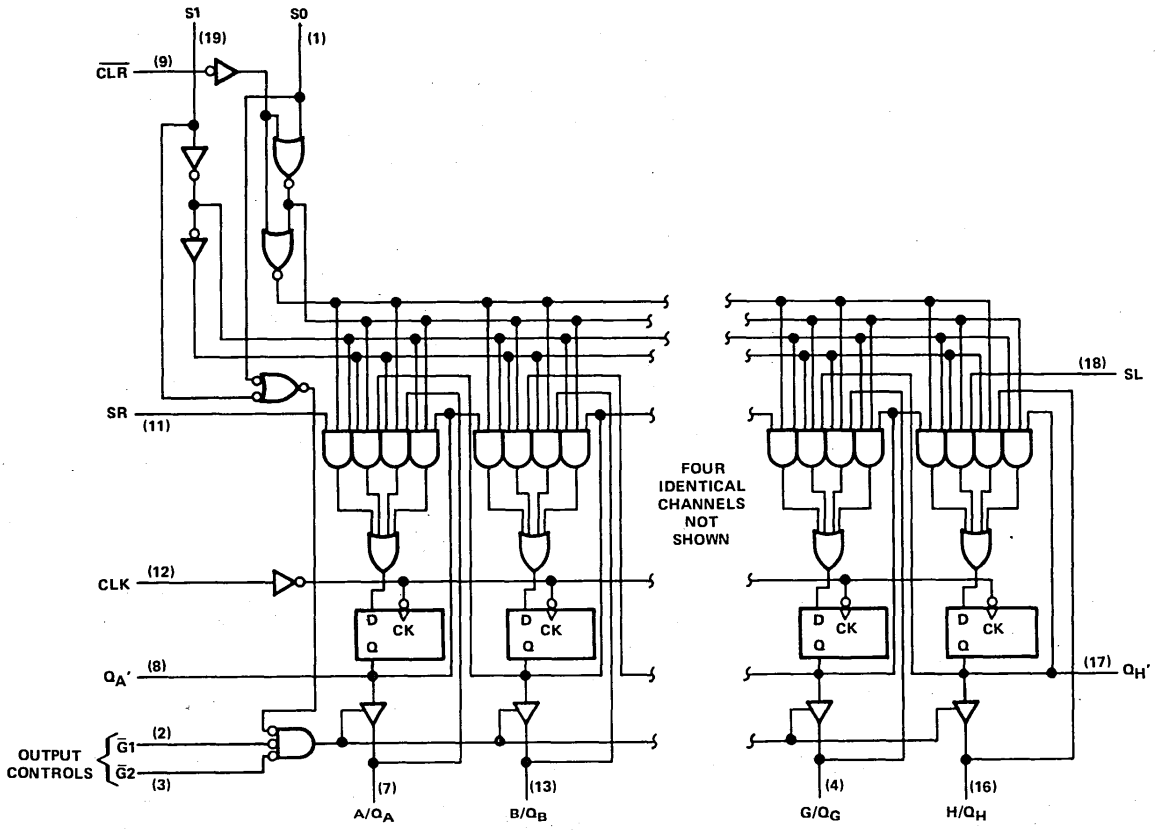
MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	$\overline{CLR}$	FUNCTION SELECT		OUTPUT CONTROL		CLK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	↑	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic diagram



INPUTS/OUTPUTS NOT SHOWN:
(6) C/Q_C (5) E/Q_E
(14) D/Q_D (15) F/Q_F

Pin numbers shown on logic notation are for DW, J or N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

schematics of inputs and outputs, absolute maximum ratings, recommended operating conditions, and electrical characteristics

Same as SN54LS299 and SN74LS299,

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 1	25	35		MHz
t_{PLH}	CLK	Q_A' or Q_H'	C_L = 15 pF, R_L = 2 kΩ		22	33	ns
t_{PHL}					26	39	
t_{PLH}	CLK	Q_A thru Q_H	C_L = 45 pF, R_L = 665 Ω		17	25	ns
t_{PHL}					25	39	
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			14	21	ns
t_{PZL}					20	30	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	C_L = 5 pF, R_L = 665 Ω		10	20	ns
t_{PLZ}					10	15	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

NOTE 1: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See General Information Section for load circuits and voltage waveforms.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265