SERIES 54/74, 54S/74S
PROGRAMMABLE READ-ONLY MEMORIES

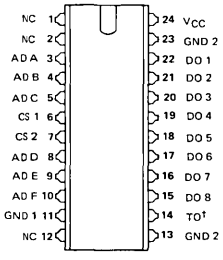
BULLETIN NO. DL-S 7512258, MAY 1975

- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  - Fast Chip Select to Simplify System Decode
  - Choice of Three-State or Open-Collector Outputs
  - P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE	OUTPUT	TYPICAL ACCESS TIME (ns)	
–55°C to 125°C	0°C to 70°C	(ORGANIZATION)	CONFIGURATION	FROM ADDRESS	FROM CHIP SELECT
SN54186(J, W)	SN74186(J, N)	512 bits (64 W x 8 B)	open-collector	50	55
SN54188A(J, W)	SN74188A(J,N)	256 bits (32 W x 8 B)	open-collector	30	34
SN54S188(J, W)	SN74S188(J, N)		open-collector	25	12
SN54S288(J, W)	SN74S288(J, N)		three-state	25	12
SN54S287(J, W)	SN74S287(J, N)	1024 bits (256 W x 4 B)	three-state	42	15
SN54S387(J, W)	SN74S387(J, N)		open-collector	42	15
SN54S470(J)	SN74S470(J, N)	2048 bits (256 W x 8 B)	open-collector	50	20
SN54S471(J)	SN74S471(J, N)		three-state	50	20
SN54S472(J)	SN74S472(J, N)	4096 bits (512 W x 8 B)	three-state	55	20
SN54S473(J)	SN74S473(J, N)		open-collector	55	20

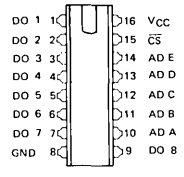
4

512 BITS (64 WORDS BY 8 BITS) '186

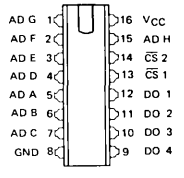


NC–No internal connection
†TO is used for testing purposes. The logic at TO is undefined.

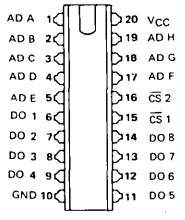
256 BITS (32 WORDS BY 8 BITS) '188A, 'S188, 'S288



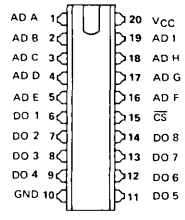
1024 BITS (256 WORDS BY 4 BITS) 'S287, 'S387



2048 BITS (256 WORDS BY 8 BITS) 'S470, 'S471



4096 BITS (512 WORDS BY 8 BITS) 'S472, 'S473



Pin assignments for all of these memories are the same for all packages.

description

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in one millisecond or less. The Schottky-clamped versions of these PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit PROM's can be used to significantly improve system density for fixed memories as all are offered in the 20-pin dual-in-line package having pin-row spacings of 0.300 inch.

description (continued)

Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387, are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

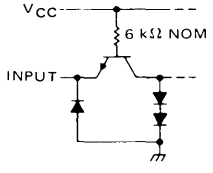
A low level at the chip-select input(s) enables each PROM except the '186, which is enabled by a high level at both chip-select inputs. The opposite level at any chip-select input causes the outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs

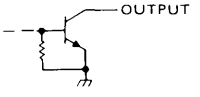
'186, '188A

EQUIVALENT OF EACH INPUT



'186, '188A

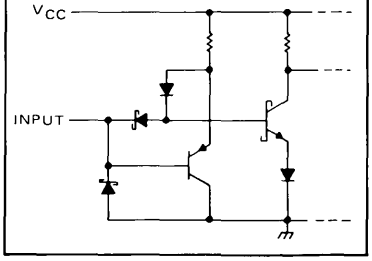
TYPICAL OF ALL OUTPUTS



Programming circuit not shown

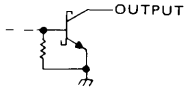
'S188, 'S287, 'S288, 'S387
'S470, 'S471, 'S472, 'S473

EQUIVALENT OF EACH INPUT



'S188, 'S387,
'S470, 'S473

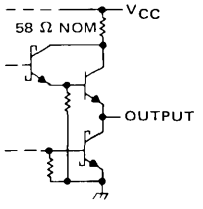
TYPICAL OF ALL OUTPUTS



Programming circuit not shown

'S287, 'S288
'S471, 'S472

TYPICAL OF ALL OUTPUTS



Programming circuit not shown

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54', SN54S' Circuits	−55°C to 125°C
SN74', SN74S' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal (GND 2 of '186),. For '186 GND 1 and both GND 2 terminals are all connected to system ground except during programming. The supply-voltage rating does not apply during programming of the '188, '188A, or the 54S/74S PROM's.

recommended conditions for programming

		MIN	NOM	MAX	UNIT
Supply voltages (see Note 2)	V_{CC}	4.75	5	5.25	V
	GND 1	−5		−6†	
Input conditions (see Note 3 and 4)	High level	Open circuit or equivalent			
	Low level	−5		−6†	V
Output voltage				−6.5†‡	V
Output current, output being programmed		−95	−120	−130	mA
Duration of programming pulse (see Note 5)		1		20	ms
Programming duty cycle			25	35	%
Free-air temperature		0		55	°C

†Absolute maximum ratings. ‡Clamp to ensure output does not exceed −0.5 V with respect to GND 1.

NOTES: 2. Voltage values are with respect to the GND 2 terminals.
3. The high-level (off) output of a Series 54/74 or 54S/74S open-collector gate with no pull-up resistor meets the requirements for a high-level input condition.
4. The low-level input voltage must be within ±0.5 volts of the applied voltage at GND 1.
5. Programming is guaranteed if the pulse is applied to the output for 10 ms. Typically, programming occurs in less than 1 ms.

step-by-step programming procedure

Programming the SN54186 or SN74186 is performed individually for each of the 512 bit locations and consists basically of applying a current pulse to each output terminal where a low logic level is to be changed to a high (off) level. The power supply and ground connections described below are designed to ensure that alteration of the memory content occurs during the programming procedure only.

1. Connect the memory as shown in Figure 1. To address a particular word in the memory, set the input switches to the binary equivalent of that word where a low logic level is as specified under "recommended conditions for programming" and a high logic level is either an open circuit or connection to an open-collector TTL gate with no pull-up resistor.
2. Apply a programming current pulse as specified to the pin associated with the first bit to be changed from a low-level to a high-level output.
3. Repeat Step 2 for each high-level output desired in the word addressed (program only one bit at a time). Any bit that is to remain at a low level should have its respective output open-circuited during the entire programming cycle for the addressed word.
4. Set the next input address and repeat steps 2 and 3 at a programming duty cycle of 35% maximum. This procedure is repeated for each input address for which a specific output word pattern is desired. A low logic level can always be changed to a high logic level simply by repeating Steps 1 and 2. Once programmed to provide a high logic level, the output cannot be changed to supply a low logic level.

NOTE: When verification indicates that a bit did not program, repeat steps 2 through 4. If the bit did not program after the second application of a 1-millisecond programming pulse, repeat steps 2 through 4 using programming pulse time of 10 to 20 milliseconds. Regardless of the programming pulse duration, its total average pulse time should be no more than 35% of the programming cycle.

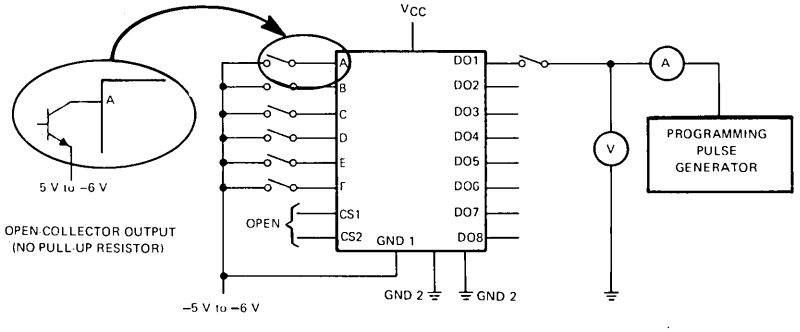


FIGURE 1—PROGRAMMING CONNECTIONS

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended conditions for programming

		'188A			SN54S', SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 6)	Steady state	4.75	5	5.75	4.75	5	5.75	V
	Program pulse	10	10.5	11†	10	10.5	11†	
Input voltage	High level, V_{IH}	2.4		5	2.4		5	V
	Low level, V_{IL}	0		0.5	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 2)			See load circuit (Figure 2)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 7)			0.25	+0.3 −0.8	0	0.25	0.3	V
Duration of V_{CC} programming pulse Y (see Figure 3 and Note 8)		1		20	1		20	ms
Programming duty cycle			25	35		25	35	%
Free-air temperature		0		55	0		55	°C

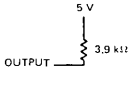
†Absolute maximum ratings.

NOTES: 6. Voltage values are with respect to the GND 2 terminals.
7. The '188A, 'S188, 'S288, 'S470, 'S471, 'S472, and 'S473 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
8. Programming is guaranteed if the pulse applied is 10 ms long. Typically, programming occurs in 1 ms.

step-by-step programming procedure

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9 kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current out of the programming output supply during programming is 150 mA.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 10 μs and 1 ms after V_{CC} has reached its 10.5-V level. See programming sequence of Figure 3.
7. After the X pulse time (1 ms) is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within 10 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.

NOTES: A) V_{CC} should be removed between program pulses to reduce dissipation and chip temperatures. See Figure 3.
B) When verification indicates that a bit did not program, repeat steps 3 through 9. If the bit did not program after the second application of a 1-ms X pulse, repeat steps 3 through 9 using an X pulse time of 10 to 20 ms. Regardless of the X duration, the total average pulse time of Y should be no more than 35% of the programming cycle.



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION
FIGURE 2

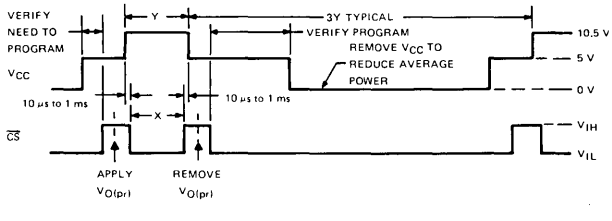


FIGURE 3–VOLTAGE WAVEFORMS FOR PROGRAMMING

recommended operating conditions

	SN54186 SN54188A			SN74186 SN74188A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'186			'188A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			100				μA
			V_{OH} = 5.5 V			200			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 12 mA				0.4			0.45	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1			−1	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 9	Both CS at 0 V		47	95				mA
			Both CS at 4.5 V		80	120				
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX	See Note 10					50	80	mA
I_{CCL}	Supply current, all outputs low		See Note 11					82	110	
C_o	Off-state output capacitance	V_{CC} = 5 V, V_O = 2 V, f = 1 MHz			6.5			6.5		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 9. I_{CC} of '186 is measured with all outputs open and the address inputs at 4.5 V. Typical values are for 50% of the bits programmed.
10. I_{CCH} of '188A is measured with all inputs at 4.5 V, all outputs open.
11. I_{CCL} of '188A is measured with the chip-select input grounded, all other inputs at 4.5 V, and all outputs open. The typical value shown is for the worst-case condition of all eight outputs low at one time. This condition may not be possible after the device has been programmed.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(CS/\overline{CS})}$ (ns) Access time from chip select (enable time)		t_{PLH} (ns) Propagation delay time, low-to-high-level output from chip select (disable time)	
		TYP	MAX	TYP	MAX	TYP	MAX
'186	C_L = 30 pF, R_{L1} = 400 Ω,	50	75	55	75	40	75
'188A	R_{L2} = 600 Ω, See Figure 4	30	50	34	50	23	50

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

		'S188			'S387, 'S470, 'S473			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				20			16	mA
Operating free-air temperature, T_A	Series 54S	−55		125	−55		125♦	°C
	Series 74S	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V				50	μA
			V_{OH} = 5.5 V				100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−250	μA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 12		'S188		80	110	mA
				'S387		100	135	
				'S470		110	155	
				'S473		120		

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{CS})}$ (ns) Access time from chip select (enable time)		t_{PLH} (ns) Propagation delay time, low-to-high-level output from chip select (disable time)	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MAX
SN54S188	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 4	25	50	12	30	12	30
SN74S188		25	40	12	25	12	25
SN54S387		42	75	15	40ʄ	15	40ʄ
SN74S387		42	65	15	35	15	35
SN54S470		50	80	20	40	15	35
SN74S470		50	70	20	35	15	30
SN54S473		55		20		15	
SN74S473		55		20		15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦An SN54S387 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 42 °C/W.
ʄTentative specifications.
NOTE 12: The typical values of I_{CC} shown are with all outputs low.

recommended operating conditions

		'S287 'S471, 'S472			'S288			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	Series 54S			−2			−2	mA
	Series 74S			−6.5			−6.5	
Low-level output current, I_{OL}				16			20	mA
Operating free-air temperature, T_A	Series 54S	−55		125	−55		125♦	°C
	Series 74S	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S'			SN74S'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 12	'S287		100	135		100	135	mA
			'S288		80	110		80	110	
			'S471		110	155		110	155	
			'S472		120			120		

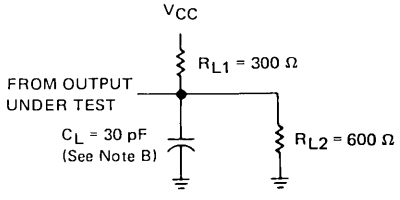
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{CS})}$ (ns) Access time from chip select (enable time)		t_{PXZ} (ns) Disable time from high or low level	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MAX
SN54S287	C_L = 30 pF for $t_{a(ad)}$ and $t_{a(\overline{CS})}$, 5 pF for t_{PXZ}; R_L = 300 Ω; See Figure 5	42	75ϕ	15	40ϕ	12	
SN74S287		42	65	15	35	12	
SN54S288		25	50	12	30	8	30
SN74S288		25	40	12	25	8	20
SN54S471		50	80	20	40	15	35
SN74S471		50	70	20	35	15	30
SN54S472		55		20		15	
SN74S472		55		20		15	

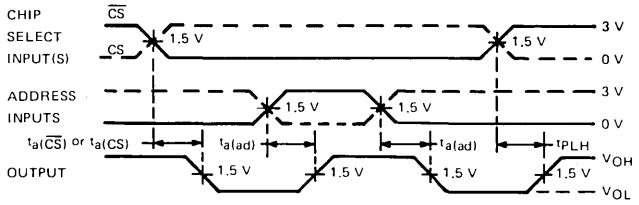
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
♦An SN54S287 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 12: The typical values of I_{CC} shown are with all outputs low.
ϕTentative specifications

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION



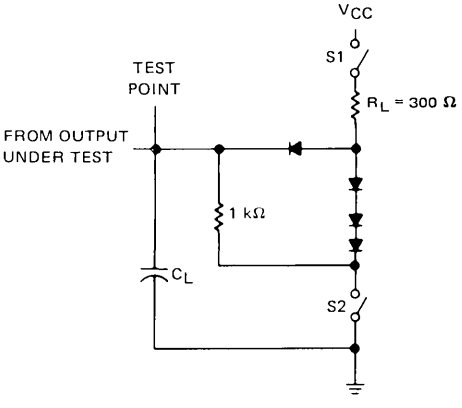
LOAD CIRCUIT



VOLTAGE WAVEFORMS

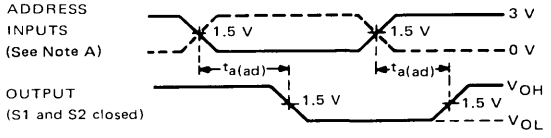
NOTES: A. The input pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR ⩽ 1 MHz. For Series 54/74, $t_r \leqslant 7$ ns, $t_f \leqslant 7$ ns. For Series 54S/74S, $t_r \leqslant 2.5$ ns, $t_f \leqslant 2.5$ ns.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 4–SWITCHING TIMES OF '186, '188A, 'S188, 'S470, 'S387, AND 'S473

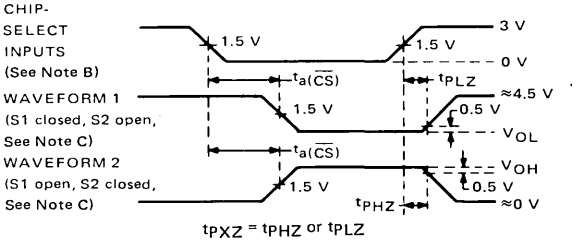


C_L includes probe and jig capacitance.
All diodes are 1N3064.

LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS
VOLTAGE WAVEFORMS



$t_{PXZ} = t_{PHZ}$ or t_{PLZ}

ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP SELECT
VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the chip-select input(s) is(are) low.
B. When measuring access and disable times from chip-select input(s), the address inputs are steady-state.
C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leqslant 2.5$ ns, $t_f \leqslant 2.5$ ns, PRR ⩽ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

FIGURE 5–SWITCHING TIMES OF 'S287, 'S288, 'S471, AND 'S472

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222