SN54180, SN74180 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

DECEMBER 1972-REVISED MARCH 1988

EU					SN54180 J OR W PACKAGE SN74180 N PACKAGE (TOP VIEW)
	UTS			UTS	
Σ OF H's AT A THRU H	EVEN	ODD	Σ EVEN	Σ ODD	$\begin{array}{ccc} G & \Box^{1} & \bigcirc 14 \Box & V_{CC} \\ H & \Box^{2} & 13 \Box & F \\ \end{array}$
EVEN	н	L	н	L	EVEN $\begin{bmatrix} 3 \\ 2 \end{bmatrix}$ E
ODD	н	L	L	н	
EVEN	L	н	L	н	
ODD	Ł	н	н	L	ΣΟΟΟ 🛛 6 🤤 Β
x	н	н	L	L	
х	L	L	н	н	

description

These universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generators/checkers, utilize familiar Series 54/74 TTL circuitry and feature odd/even outputs and control inputs to facilitate operation in either odd or even-parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

The SN54180/SN74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of -55° C to 125° C; and the SN74180 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	Supply voltage, V _{CC} (see Note 1)																	7	v
	Input voltage																	5.5	V
	Operating free-air temperature range: SN54180 Circuits												•		-	-55°	'C to	<mark>ه 125 م</mark>	C
	SN74180 Circuits																		
	Storage temperature range		•	•		•	•	•	•	•	•	•	•	•	-	-65	'C to	o 150°	C
NOT	E 1: Voltage values are with respect to network ground terminal.																		

recommended operating conditions

		SN5418	0				
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH			-800			-800	μA
Low-level output current, IOL			16			16	mA
Operating free-air temperature, T _A	-55		125	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETE	P	TEST CONDITIONS [†]	L	SN5418	0		1		
	FARAMETE	.n	TEST CONDITIONS:	MIN	түр‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.8		•	0.8	V
VIK	Input clamp voltage		$V_{CC} = MIN$, $I_I = -12 \text{ mA}$			-1.5	-		-1.5	v
v _{он}	High-level output voltage	3	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 μA	2.4	3.3		2.4	3.3		v
V _{OL}	Low-level output voltage	•	$V_{CC} = MIN, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OL} = 16 mA$		0.2	0.4		0.2	0.4	v
lj –	Input current at maximu	im input voltage	V _{CC} = MAX, V _I = 5.5 V			1		_	1	mA
ηн	High-level input current	Any data input	Vcc = MAX, VI = 2.4 V			40			40	
н	ingn-ever input current	Even or odd input				80			80	μA
LIL.	Low-level input current	Any data input	V _{CC} = MAX, V _I = 0.4 V			-1.6			-1.6	
'IL		Even or odd input	VCC - MAX; V1 - 0.4 V			-3.2			-3.2	mA
los	Short-circuit output curr	ent §	V _{CC} = MAX	-20		-55	-18		-55	mA
lcc	Supply current		V _{CC} = MAX, See Note 2		34	49		34	56	mA

TTL Devices

NOTE 2: I_{CC} is measured with even and odd inputs at 4.5 V, all other inputs and outputs open.

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. [‡]All typical values are at V_{CC} = 5 V, T_A = 25°C. § Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	ТҮР	МАХ	UNIT
^t PLH	Data	Σ Even			40	60	
^t PHL		2 LVen	C _L = 15 pF, R _L = 400 s	s, 🔽	45	68	ns
^t PLH	Data	Σ Odd	Odd input grounded, See Note 3		32	48	
^t PHL	Dala	2 000			25	38	ns
^t PLH	Data	ΣEven			32	48	
tPHL	Data	2 LVen	C _L = 15 pF, R _L = 400 s	s,	25	38	ns
^t PLH	Data	Σ Odd	Even input grounded, See Note 3		40	60	
^t PHL	Duta	2 000			45	68	ns
^t PLH	Even or Odd	Σ Even or Σ Odd	$C_{L} = 15 \text{pF}, \qquad R_{L} = 400 \text{s}$	s,	13	20	
^t PHL			See Note 3		7	10	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

logic symbol[†]

na setate a tra



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.





logic diagram (positive logic)

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