GD5F4GM5xFxxG

DATASHEET

4G-bit 4KPageSize with F Version

Contents

1 FEATURE

◆ 4Gb SLC NAND Flash

◆ Organization (1)
- Internal ECC On (ECC_EN=1, default):
Page Size：4096-Byte+128-Byte
- Internal ECC Off (ECC_EN=0):
Page Size：4096-Byte+256-Byte

◆ Standard, Dual, Quad SPI
- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
- Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3

◆ High Speed Clock Frequency
- 120MHz for fast read with 30pF load
- Quad I/O Data transfer up to 480Mbits/s

◆ Software/Hardware Write Protection
- Write protect all/portion of memory via software
- Register protection with WP# Pin

◆ Advanced security Features
- 16K-Byte OTP Region
- Unique ID
- Parameter Page

◆ Single Power Supply Voltage
- Full voltage range for 1.8V: 1.7V ~ 2.0V
- Full voltage range for 3.3V: 2.7V ~ 3.6V

◆ Program/Erase/Read Speed
- Page Program time: 480us typical
- Block Erase time: 3ms typical
- Page read time: 120us maximum(w/I ECC)

◆ Low Power Consumption
- 40mA maximum active current
- 90uA maximum standby current

◆ Enhanced access performance
- 4kbyte cache for fast random read

◆ Advanced Feature for NAND
- Internal 8bit ECC per 528bytes
- Internal data move by page with ECC

◆ The first block(Block0) is guaranteed to be a valid block at the time of shipment.

Note: (1) ECC is enabled by default, which can be disabled by user.

2 GENERAL DESCRIPTION

SPI (Serial Peripheral Interface) NAND Flash provides an ultra cost-effective while high density non-volatile memory storage solution for embedded systems, based on an industry-standard NAND Flash memory core. It is an attractive alternative to SPI-NOR and standard parallel NAND Flash, with advanced features:

- Total pin count is 8, including VCC and GND
- Density 4G bit
- Superior write performance and cost per bit over SPI-NOR
- Significant low cost than parallel NAND

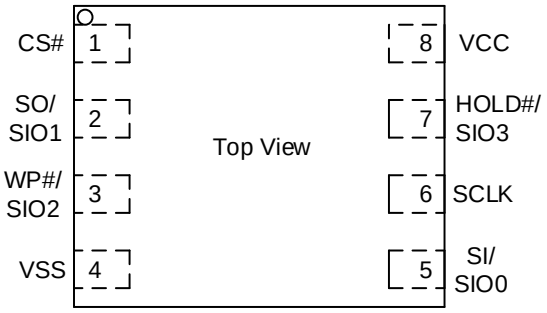
This low-pin-count NAND Flash memory follows the industry-standard serial peripheral interface, and always remains the same pinout from one density to another. The command sets resemble common SPI-NOR command sets, modified to handle NAND specific functions and added new features. GigaDevice SPI NAND is an easy-to-integrate NAND Flash memory, with specified designed features to ease host management:

- **User-selectable internal ECC**. ECC code is generated internally during a page program operation. When a page is read to the cache register, the ECC code is detect and correct the errors when necessary. The 128-bytes spare area is available even when internal ECC enabled. The device outputs corrected data and returns an ECC error status.
- **Internal data move or copy back with internal ECC**. The device can be easily refreshed and manage garbage collection task, without need of shift in and out of data.
- **Power on Read with internal ECC**. The device will automatically read first page of fist block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promised correctly by internal ECC.

It is programmed and read in page-based operations, and erased in block-based operations. Data is transferred to or from the NAND Flash memory array, page by page, to a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation. The cache register functions as the buffer memory to enable page and random data READ/WRITE and copy back operations. These devices also use a SPI status register that reports the status of device operation.

2.1 Connection Diagram

Figure 2_1.Connection Diagram



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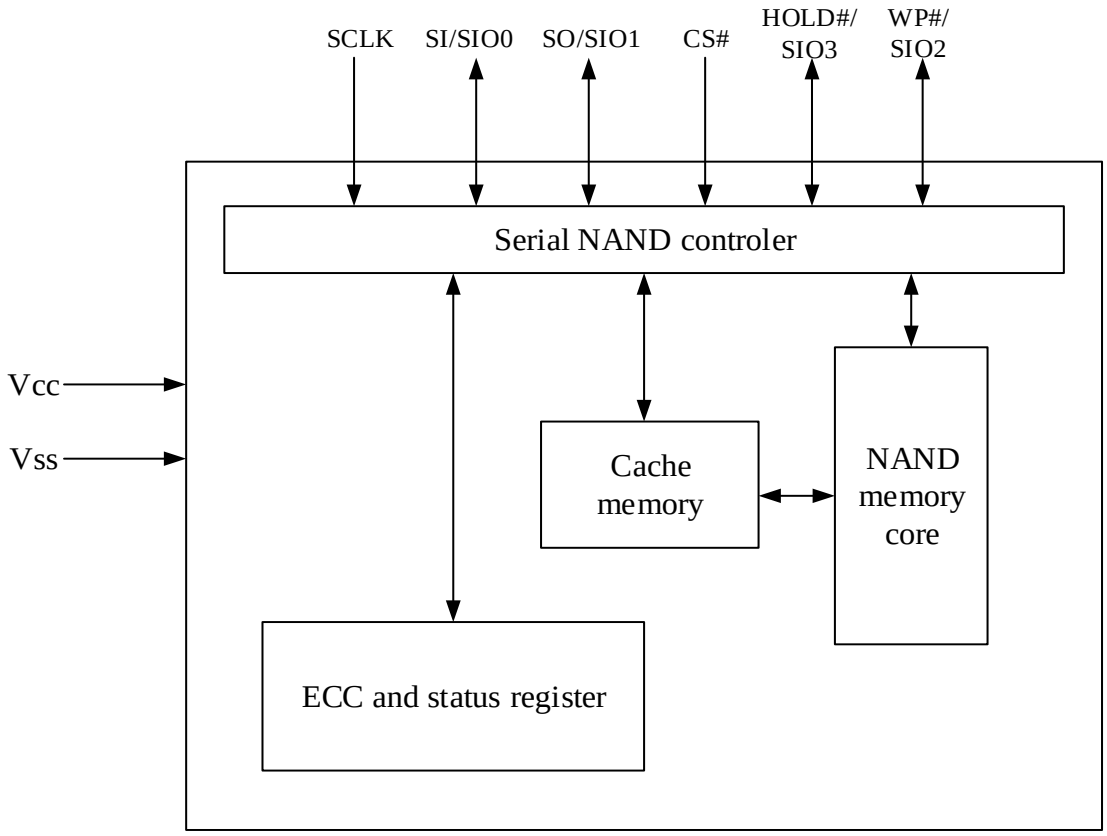
2.2 Pin Description

Table2_1.Pin Description

Pin Name	I/O	Description
CS#	**I**	Chip Select input, active low
SO/SIO1	**I/O**	Serial Data Output / Serial Data Input Output 1
WP#/SIO2	**I/O**	Write Protect, active low / Serial Data Input Output 2
VSS	**Ground**	Ground
SI/SIO0	**I/O**	Serial Data Input / Serial Data Input Output 0
SCLK	**I**	Serial Clock input
HOLD#/SIO3	**I/O**	Hold input, active low / Reset input, active low / Serial Data Input Output3
VCC	**Supply**	Power Supply
NC		Not Connect, Not internal connection; can be driven or floated.

2.3 Block Diagram

Figure 2_2. Block Diagram

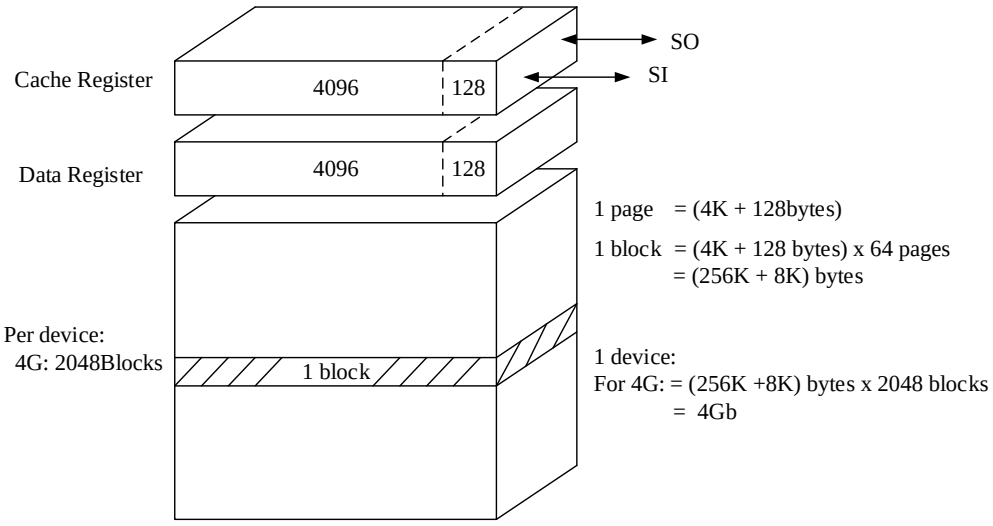


3 ARRAY ORGANIZATION

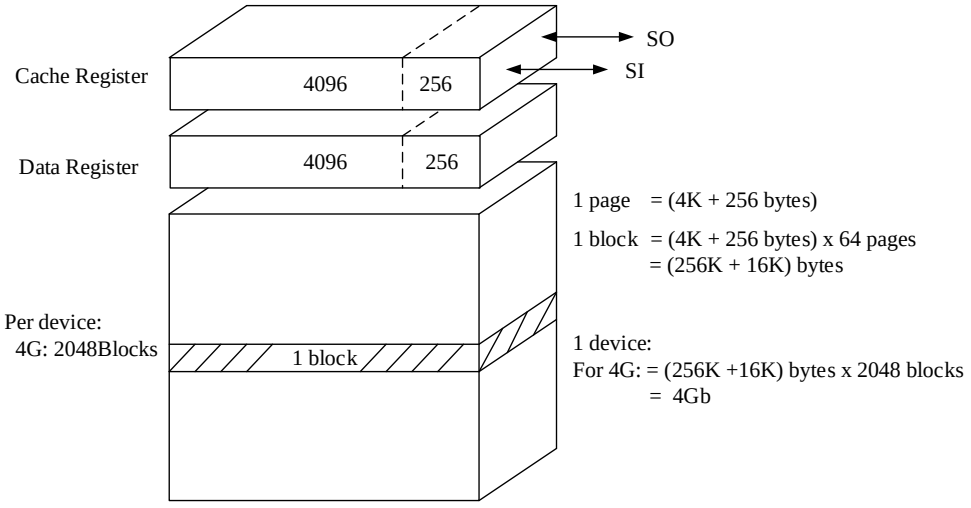
Table3. Array Organization

Each Device	Each block has	Each page has	
512M	256K	4K	bytes
2048x64	64	-	pages
2048	-	-	blocks

Figure 3. Array Organization



Internal ECC = ON



Internal ECC = OFF

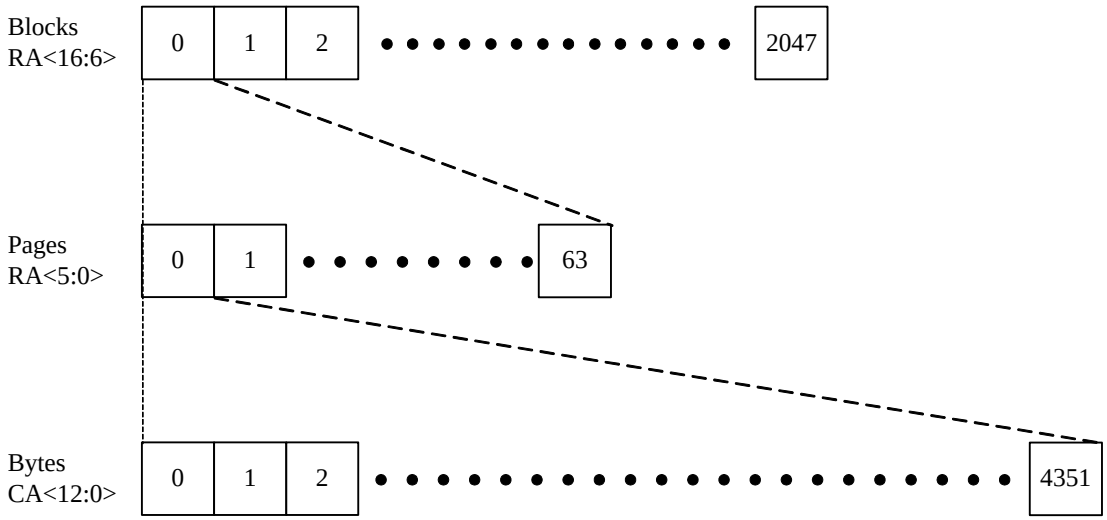
Note:

1.When Internal ECC is enabled，user can program the first 128 bytes of the entire 256 bytes spare area and the last 128 bytes of the whole spare area cannot be programed，user can read the entire 256 Byte spare area.

2.When Internal ECC is disabled，user can read and program the entire 256 bytes spare area.

4 MEMORY MAPPING

Figure 4. Array Organization



Note:

1. CA: Column Address. The 13-bit address is capable of addressing from 0 to 8191 bytes; however, only bytes 0 through 4351 are valid. Bytes 4352 through 8191 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<16:6> selects a block:

5 DEVICE OPERATION

5.1 SPI Modes

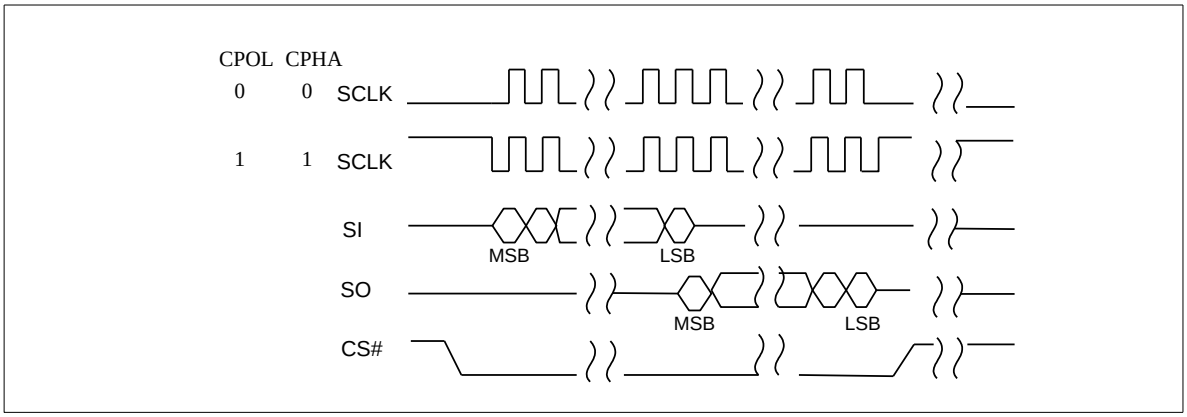
SPI NAND supports two SPI modes:

• CPOL = 0, CPHA = 0 (Mode 0)

• CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK for both modes. All timing diagrams shown in this data sheet are mode 0. See Figure 5_1 for more details.

Figure 5_1. SPI Modes Sequence Diagram



Note: While CS# is HIGH, keep SCLK at VCC or GND (determined by mode 0 or mode 3). Do not toggle SCLK until CS# is driven LOW.

We recommend that the user pull CS# to high when user don't use SPI flash, otherwise the flash is always in the read state, which is not good for flash.

When CS# is high and SCLK at VCC or GND state, the device is in idle state.

Standard SPI

SPI NAND Flash features a standard serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO).

Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1.

Quad SPI

SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1, and WP# and HOLD# pins become SIO2 and SIO3.

5.2 HOLD Mode

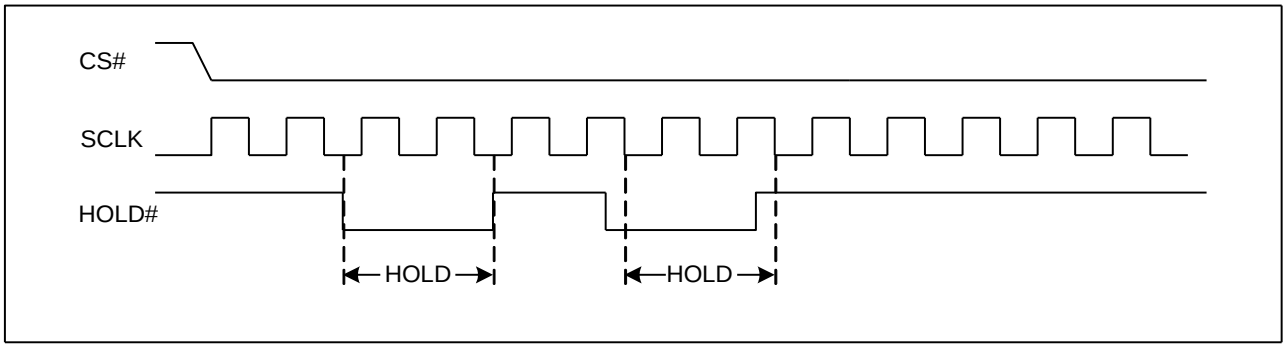
The HOLD# function is only available when QE=0, If QE=1, The HOLD# functions is disabled, the pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don't care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure 5_2. Hold Condition



5.3 Write Protection

SPI NAND provides Hardware Protection Mode besides the Software Mode. Write Protect (WP#) prevents the block lock bits (BP0, BP1, BP2 and INV, CMP) from being over written. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

To enable the Write Protection, the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

5.4 Power Off Timing

Please do not turn off the power before Write/Erase operation is completed. Avoid using the device when the battery is low. Power shortage and/or power failure before Write/Erase operation is completed will cause loss of data and/or damage to data.

6 COMMANDS DESCRIPTION

Table6. Commands Set

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte N
Write Enable	06H					
Write Disable	04H					
Get Features	0FH	A7-A0	D7-D0	Wrap(8)		
Set Feature	1FH	A7-A0	D7-D0			
Page Read (to cache)	13H	A23-A16	A15-A8	A7-A0		
Read From Cache	03H	dummy(1)	A15-A8	A7-A0(3)	D7-D0	
Fast Read From Cache	0BH	dummy(1)	A15-A8	A7-A0(3)	dummy(2)	D7-D0
Read From Cache x 2	3BH	dummy(1)	A15-A8	A7-A0(3)	dummy(2)	(D7-D0)x2
Read From Cache x 4	6BH	dummy(1)	A15-A8	A7-A0(3)	dummy(2)	(D7-D0)x4
Read ID(5)	9FH	MID	DID	DID		
Program Load	02H	A15-A8	A7-A0(4)	D7-D0	Next byte	Byte N
Program Load x4	32H	A15-A8	A7-A0(4)	(D7-D0)x4	Next byte	Byte N
Program Execute	10H	A23-A16	A15-A8	A7-A0		
Program Load Random Data	84H(7)	A15-A8	A7-A0(4)	D7-D0	Next byte	Byte N
Program Load Random Data x4	C4H/34H(7)	A15-A8	A7-A0(4)	(D7-D0)x4	Next byte	Byte N
Block Erase(256K)	D8H	A23-A16	A15-A8	A7-A0		
Reset(6)	FFH					

Notes:

1. The dummy has 8 clock.
2. The dummy has 8 clock.
   0BH/3BH/6BH has 1 byte dummy.
3. The A15-A0 (03H/0BH/3BH/6BH) has 16 clock, include 3 clock dummy.
4. The A15-A0 has 16 clock, include 3 clock dummy.
5. MID is Manufacture ID (C8h for GigaDevice), DID is Device ID.
6. Reset command:
   - Reset will reset PAGE READ/PROGRAM/ERASE operation.
   - Reset will reset status register bits P_FAIL/E_FAIL/ WEL/OIP/ECCS.
7. Those commands are only available in Internal Data Move operation.
8. The output would be updated by real-time, until CS# is driven high.
9. Please contact GD Sales for Unique ID/Parameter Page function.

7 WRITE OPERATIONS

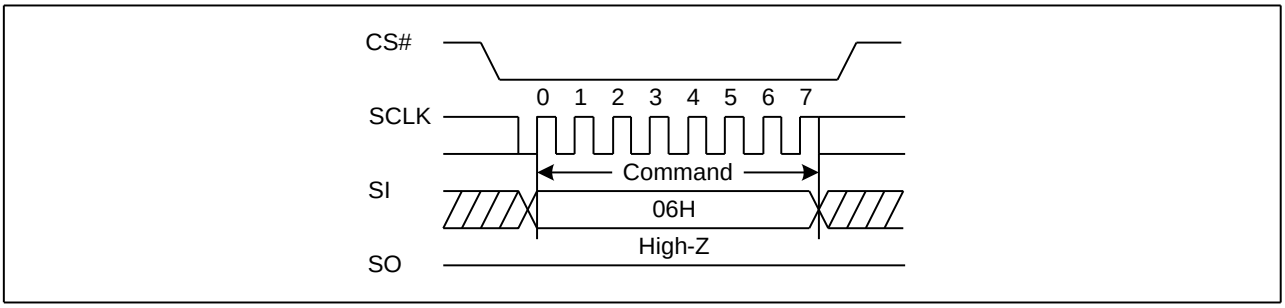
7.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to following operations that change the contents of the memory array:

- Page program
- OTP program/OTP protection
- Block erase

The WEL bit can be cleared after a reset command.

Figure 7_1. Write Enable Sequence Diagram

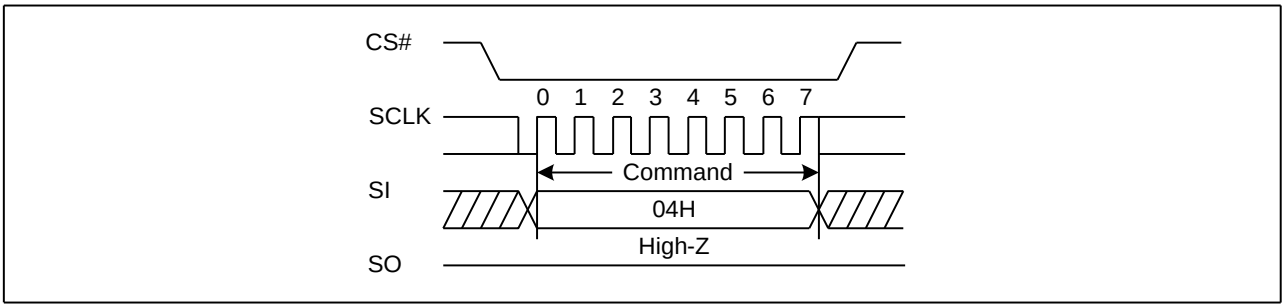


7.2 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WEL bit is reset by following condition:

- Page program
- OTP program/OTP protection
- Block erase

Figure 7_2. Write Disable Sequence Diagram



8 READ OPERATIONS

8.1 Page Read

The PAGE READ (13H) command transfers the data from the NAND Flash array to the cache register. The command sequence is as follows:

- 13H (PAGE READ to cache)
- 0FH (GET FEATURES command to read the status)
- 03H or 0BH (Read from cache)/3BH (Read from cache x2)/6BH (Read from cache x4)

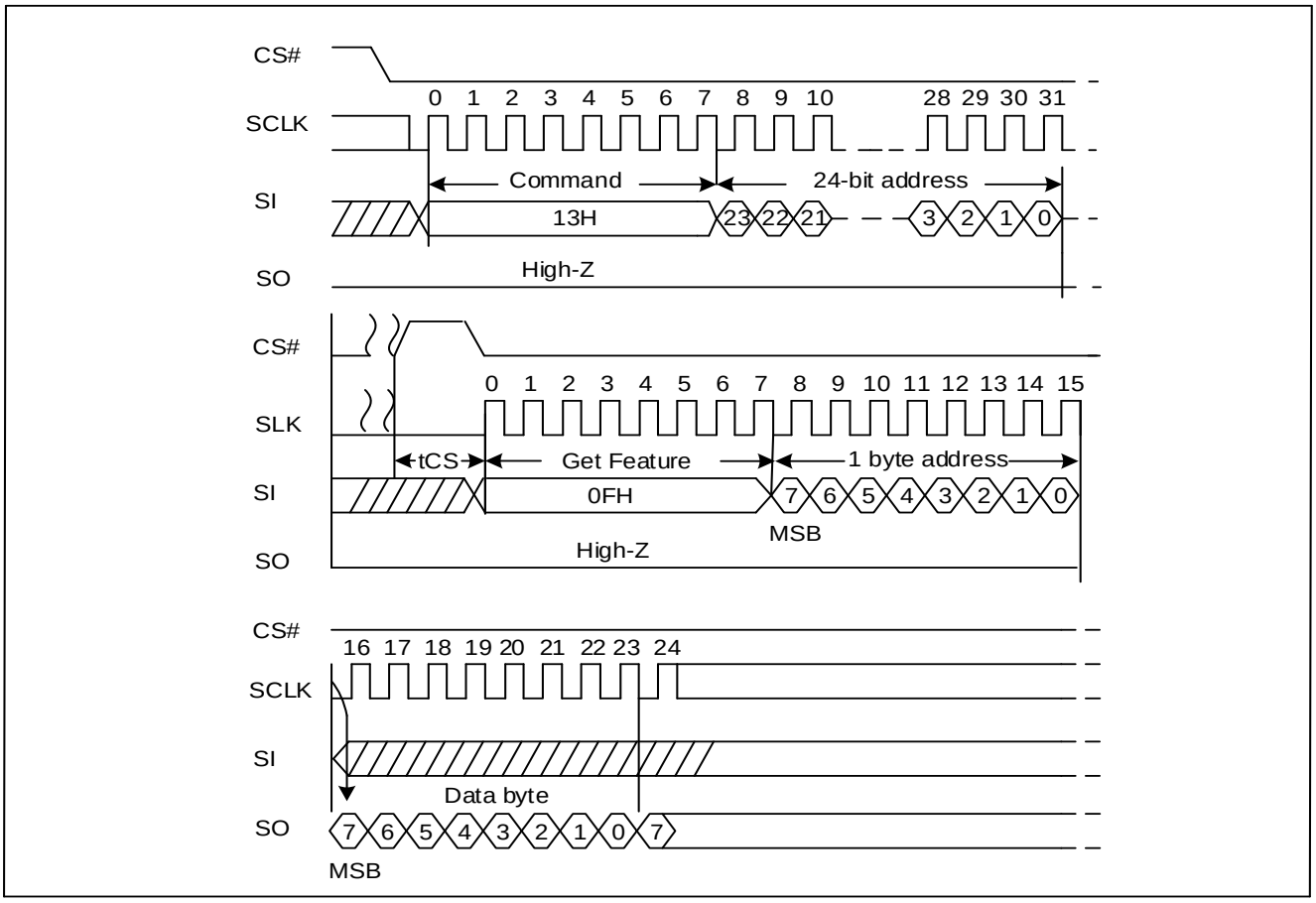
The PAGE READ command requires a 24-bit address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tRD time. During this time, the GET FEATURE (0FH) command can be issued to monitor the status. Followed the page read operation, the RANDOM DATAREAD (03H/0BH/3BH/6BH) command must be issued in order to read out the data from cache. The output data starts at the initial address specified in the command, and will continue until CS# is pulled high to terminate this operation. Refer waveforms to view the entire READ operation.

Note: The command 6BH is only available with the QE enabled.

8.2 Page Read to Cache (13H)

The command page read to cache is read the data from flash array to cache register.

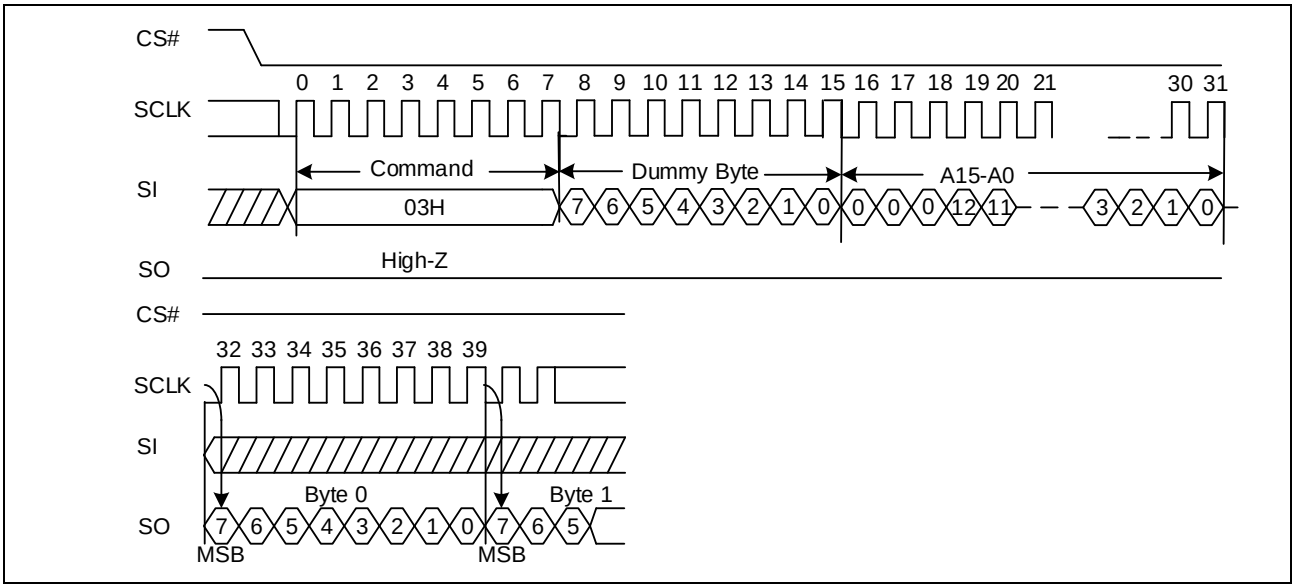
Figure 8_1.Page Read to cache Sequence Diagram



8.3 Read From Cache (03H)

The command sequence is shown below.

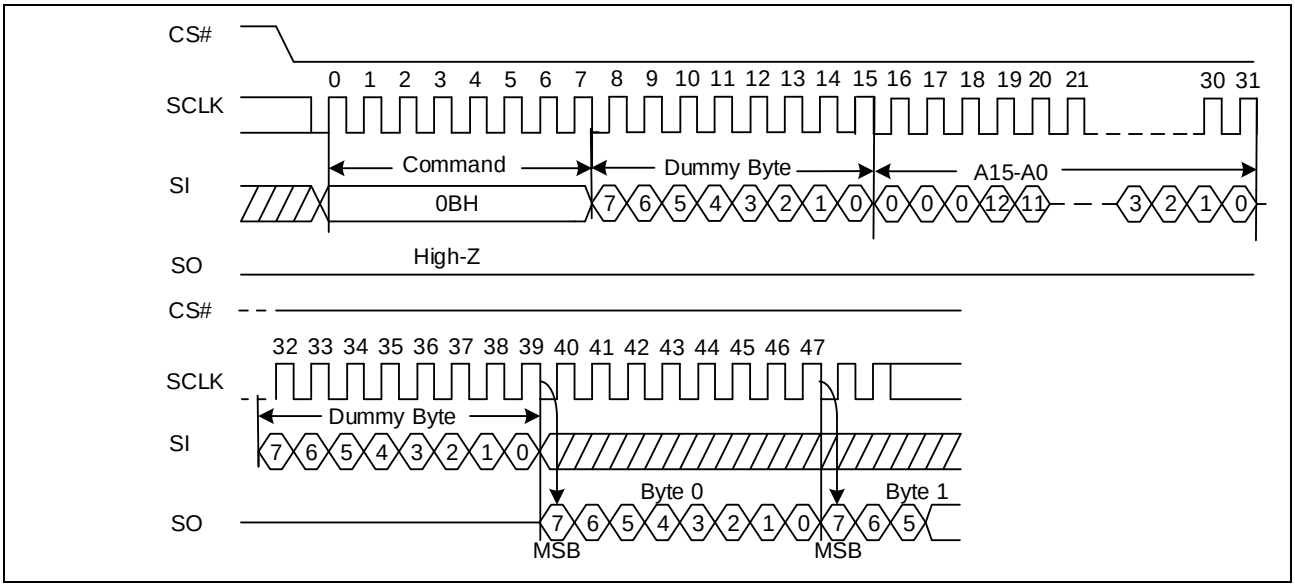
Figure 8_2. Read From Cache Sequence Diagram



8.4 Fast Read from Cache (0BH)

The command sequence is shown below.

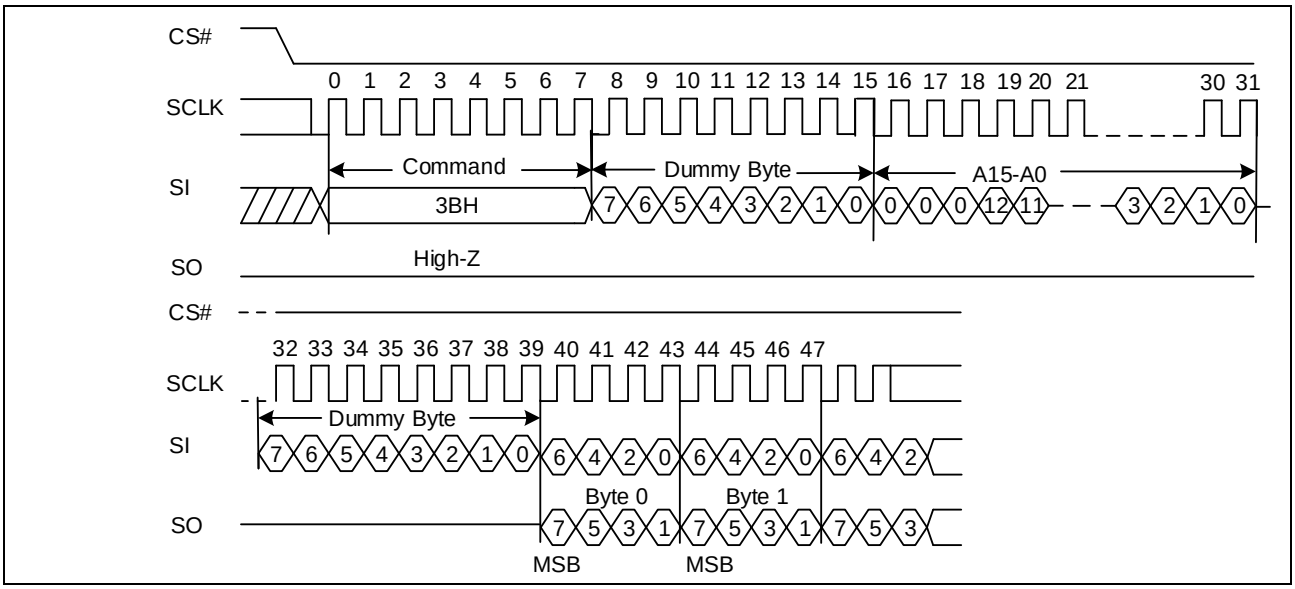
Figure 8_3. Read From Cache Sequence Diagram



8.5 Read from Cache x2 (3BH)

The command sequence is shown below.

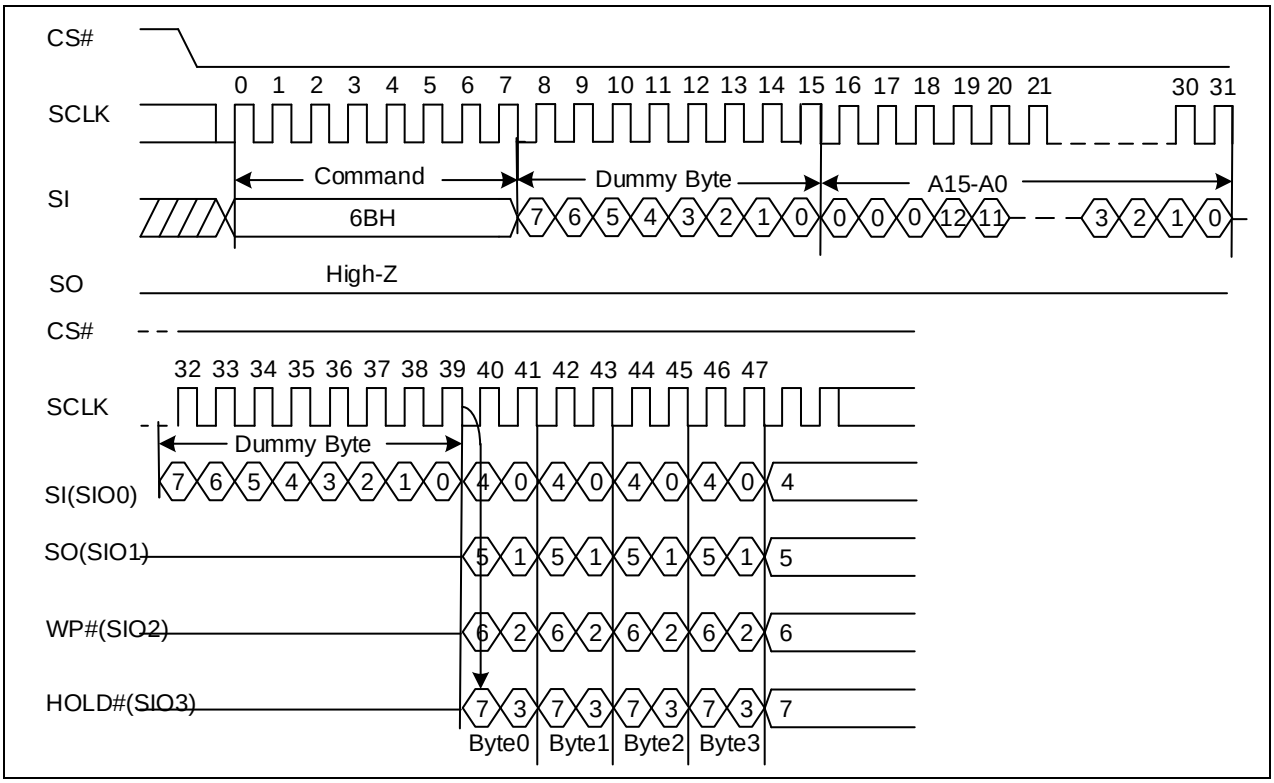
Figure 8_4. Read From Cache x2 Sequence Diagram



8.6 Read from Cache x4 (6BH)

The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache x4 command. The command sequence is shown below.

Figure 8_5. Read From Cache x4 Sequence Diagram



8.7 Read ID (9FH)

The READ ID command is used to identify the NAND Flash device.

•The READ ID command outputs the Manufacturer ID and the device ID. See Table 8_1 for details.

Figure 8_6. Read ID Sequence Diagram

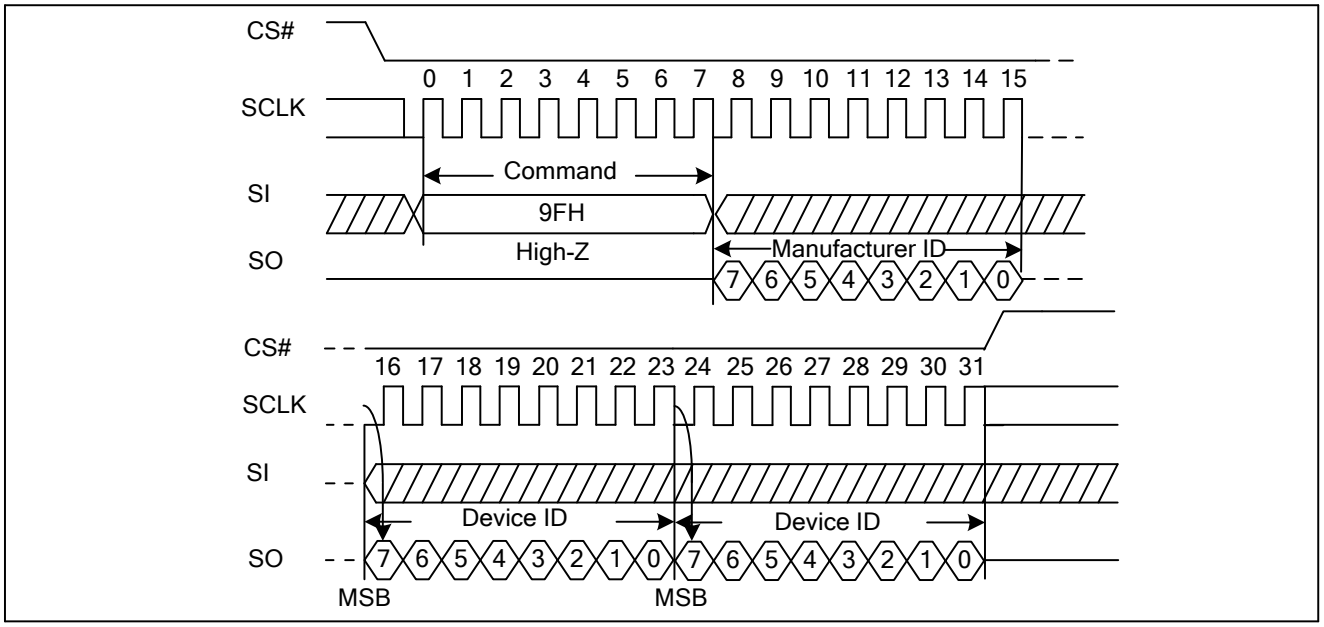


Table8_1. READ ID Table

Part No	MID	DID1	DID2
GD5F4GM5UFxxG	C8H	B4H	68H
GD5F4GM5RFxxG	C8H	A4H	68H

9 PROGRAM OPERATIONS

9.1 Page Program

The PAGE PROGRAM operation sequence programs 1 byte to whole page of data within a page. The page program sequence is as follows:

- 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

Firstly, a PROGRAM LOAD (02H/32H) command is issued. PROGRAM LOAD consists of an 8-bit Op code, followed by 3 dummy bits and a 13-bit column address, then the data bytes to be programmed. The Program address should be in sequential order in a block. The data bytes are loaded into a cache register that is whole page long. If more than one page data are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Figure 9_1 shows the PROGRAM LOAD operation. Secondly, prior to performing the PROGRAM EXECUTE operation, a WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

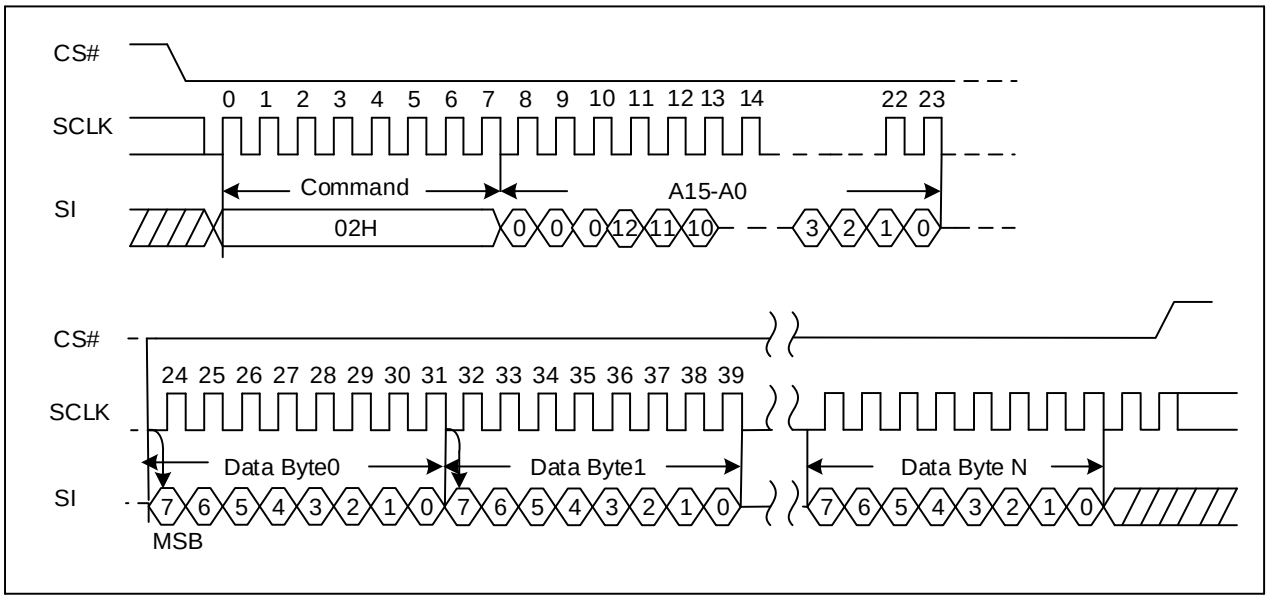
Note:

1. The contents of Cache Register doesn't reset when Program Random Load (84h) command and RESET (FFh) command.
2. When Program Execute (10h) command was issued just after Program Load (02h) command, the 0xFF is output to the address that data was not loaded by Program Load (02h) command.
3. When Program Execute (10h) command was issued just after Program Load Random Data (84h) command, the contents of Cache Register is output to the NAND array.
4. The Program address should be in sequential order in a block.
5. Program Load x4 is only available with the QE enabled.

9.2 Program Load (PL) (02H)

The command sequence is shown below.

Figure 9_1. Program Load Sequence Diagram

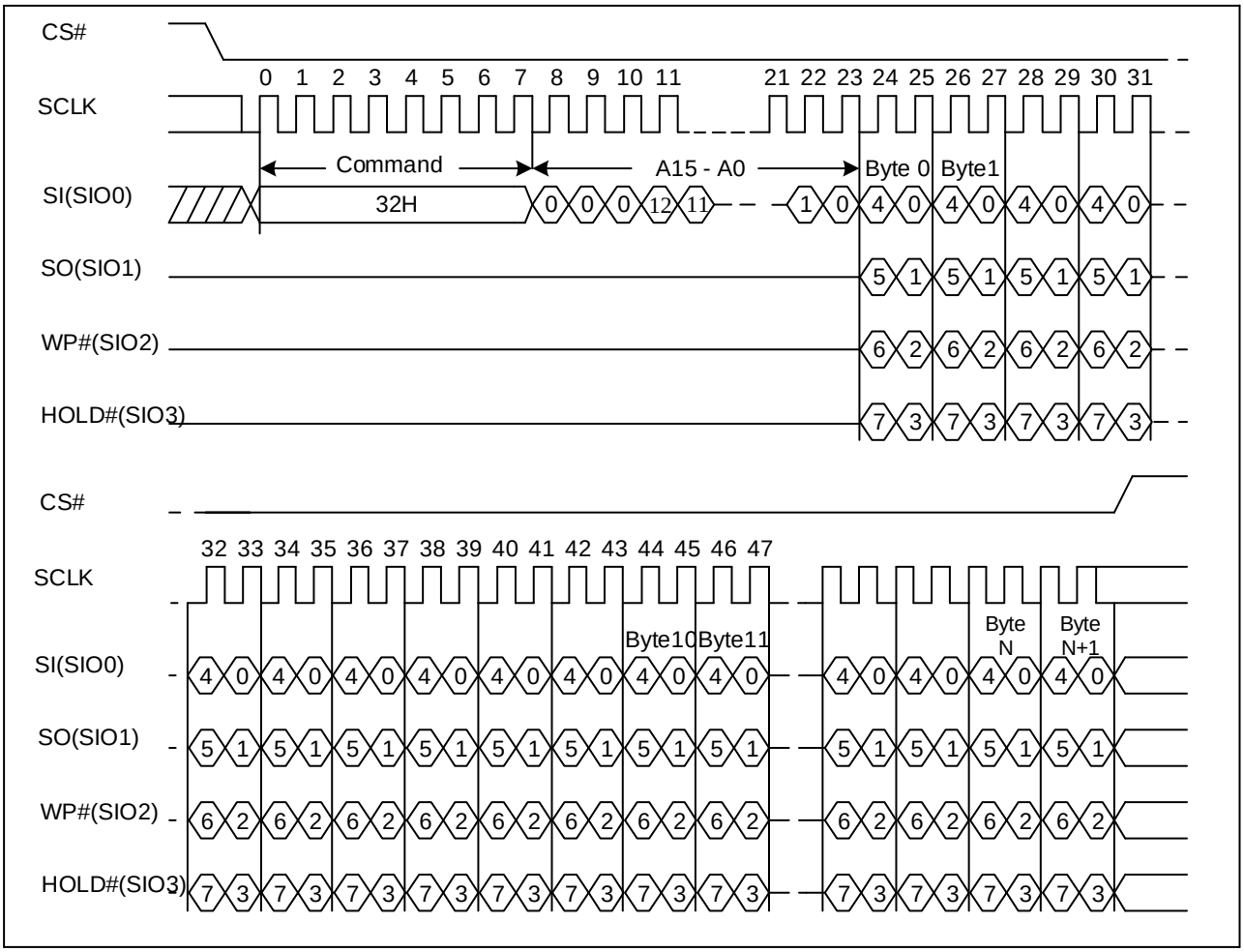


Note: When internal ECC disabled the Data Byte is 4352, when internal ECC enabled the Data Byte is 4224.

9.3 Program Load x4 (PL x4) (32H)

The Program Load x4 command (32H) is similar to the Program Load command (02H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the program load x4 command. The command sequence is shown below.

Figure 9_2. Program Load x4 Sequence Diagram

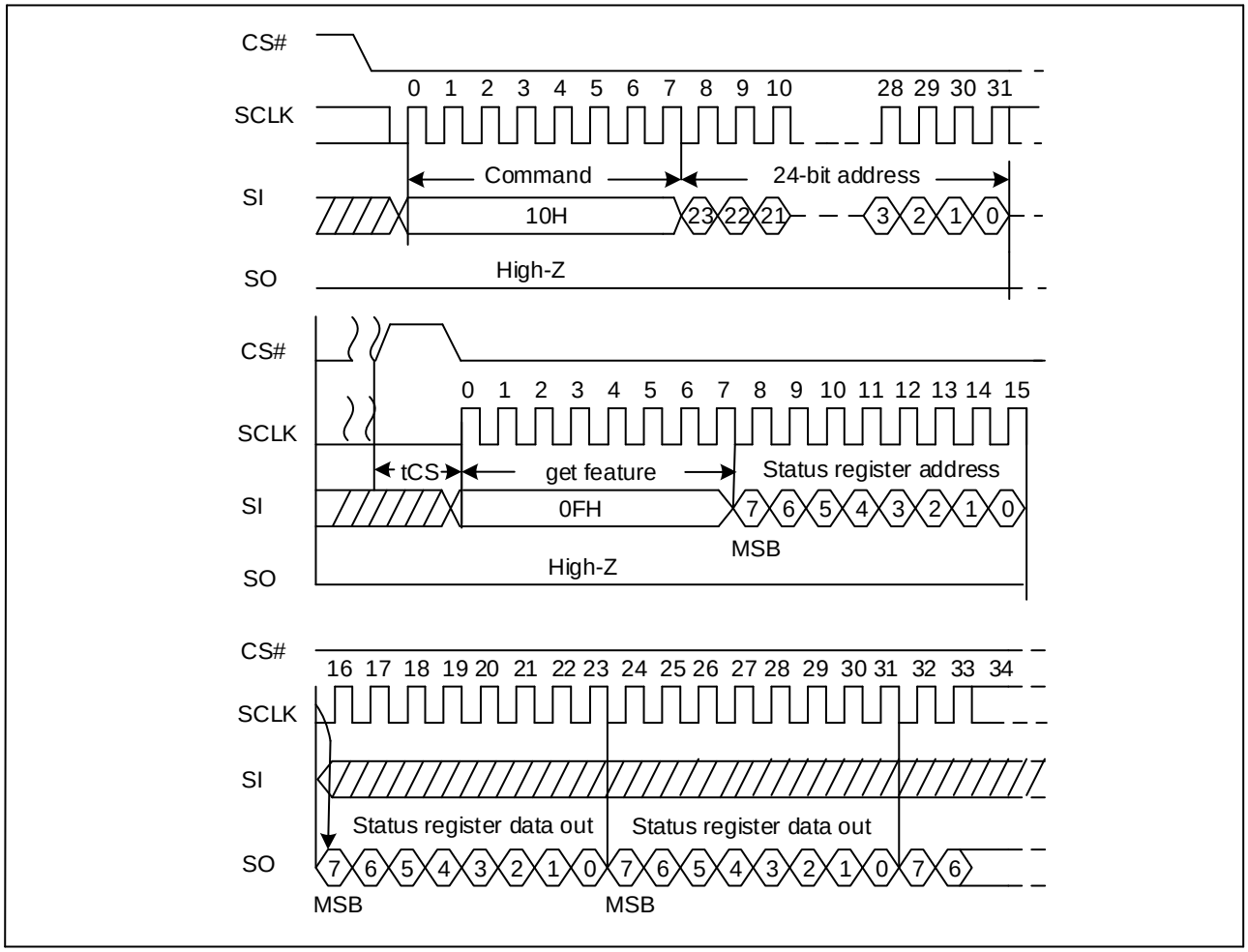


Note: When internal ECC disabled the Data Byte is 4352, when internal ECC enabled the Data Byte is 4224.

9.4 Program Execute (PE) (10H)

After the data is loaded, a PROGRAM EXECUTE (10H) command must be issued to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address. After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time. This operation is shown in Figure 9_3. During this busy time, the status register can be polled to monitor the status of the operation (refer to Status Register). When the operation completes successfully, the next series of data can be loaded with the PROGRAMLOAD command. The command sequence is shown below.

Figure 9_3. Program Execute Sequence Diagram



9.5 Internal Data Move

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

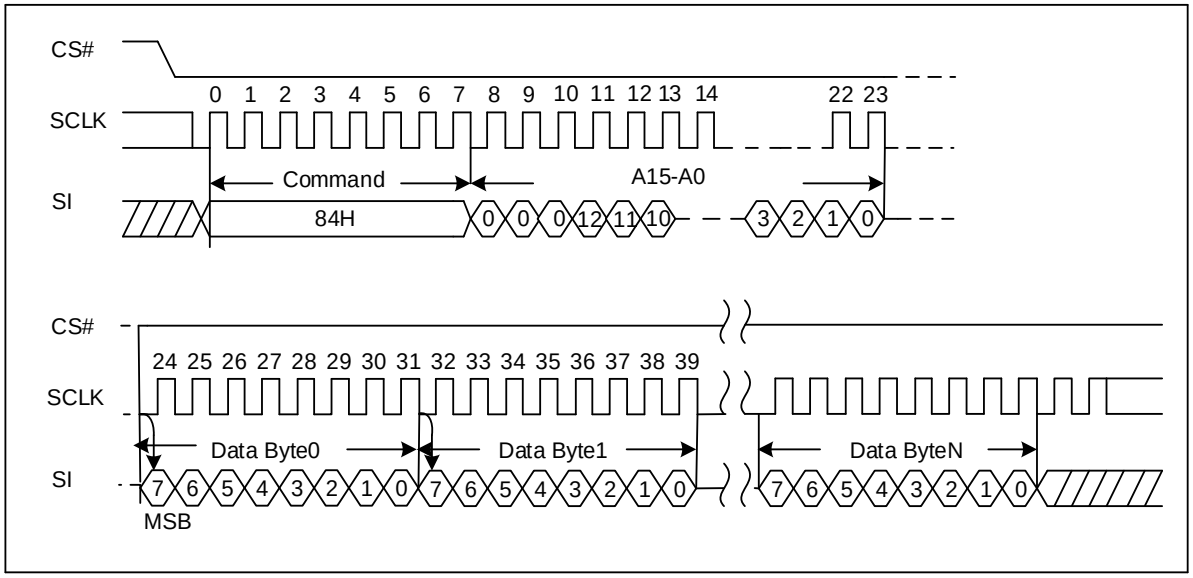
- 13H (PAGE READ to cache)
- Optional 84H/C4H/34H (PROGRAM LOAD RANDOM DATA)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a PAGE READ (13H) command. The PROGRAM LOAD RANDOM DATA (84H/C4H/34H) command can be issued, if user wants to update bytes of data in the page. New data is loaded in the 13-bit column address. If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84H/C4H/34H) command must be issued with the new column address. After the data is loaded, the WRITE ENABLE command must be issued, and then PROGRAM EXECUTE (10H) command can be issued to start the programming operation. Only the block with the same parity attribute can use the command.

9.6 Program Load Random Data (84H)

This command consists of an 8-bit Op code, followed by 3 dummy bits and a 13-bit column address. New data is loaded in the column address provided with the 13 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84H) command must be issued with a new column address, see Figure9_4 for details. This command is only available during internal data move sequence.

Figure 9_4. Program Load Random Data Sequence Diagram

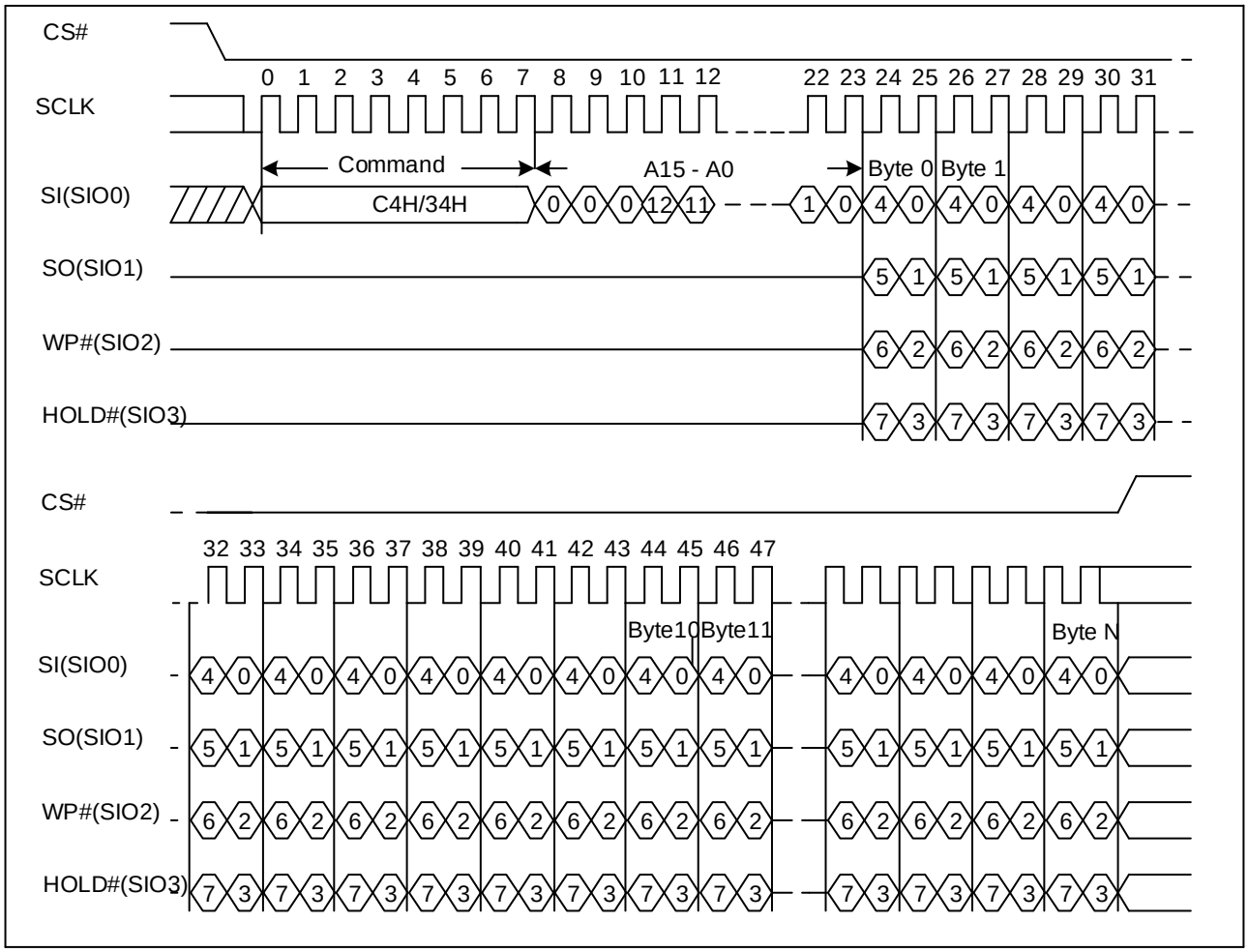


Note: when internal ECC disabled the Data Byte is 4352, when internal ECC enabled the Data Byte is 4224.

9.7 Program Load Random Data x4 (C4H/34H)

The Program Load Random Data x4 command (C4H/34H) is similar to the Program Load Random Data command (84H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable for the program load random data x4 command. See Figure 9_5 for details. Those two commands are only available during internal data move sequence.

Figure 9_5. Program Load Random Data x4 Sequence Diagram



Note: when internal ECC disabled the Data Byte is 4352, when internal ECC enabled the Data Byte is 4224.

10 ERASE OPERATIONS

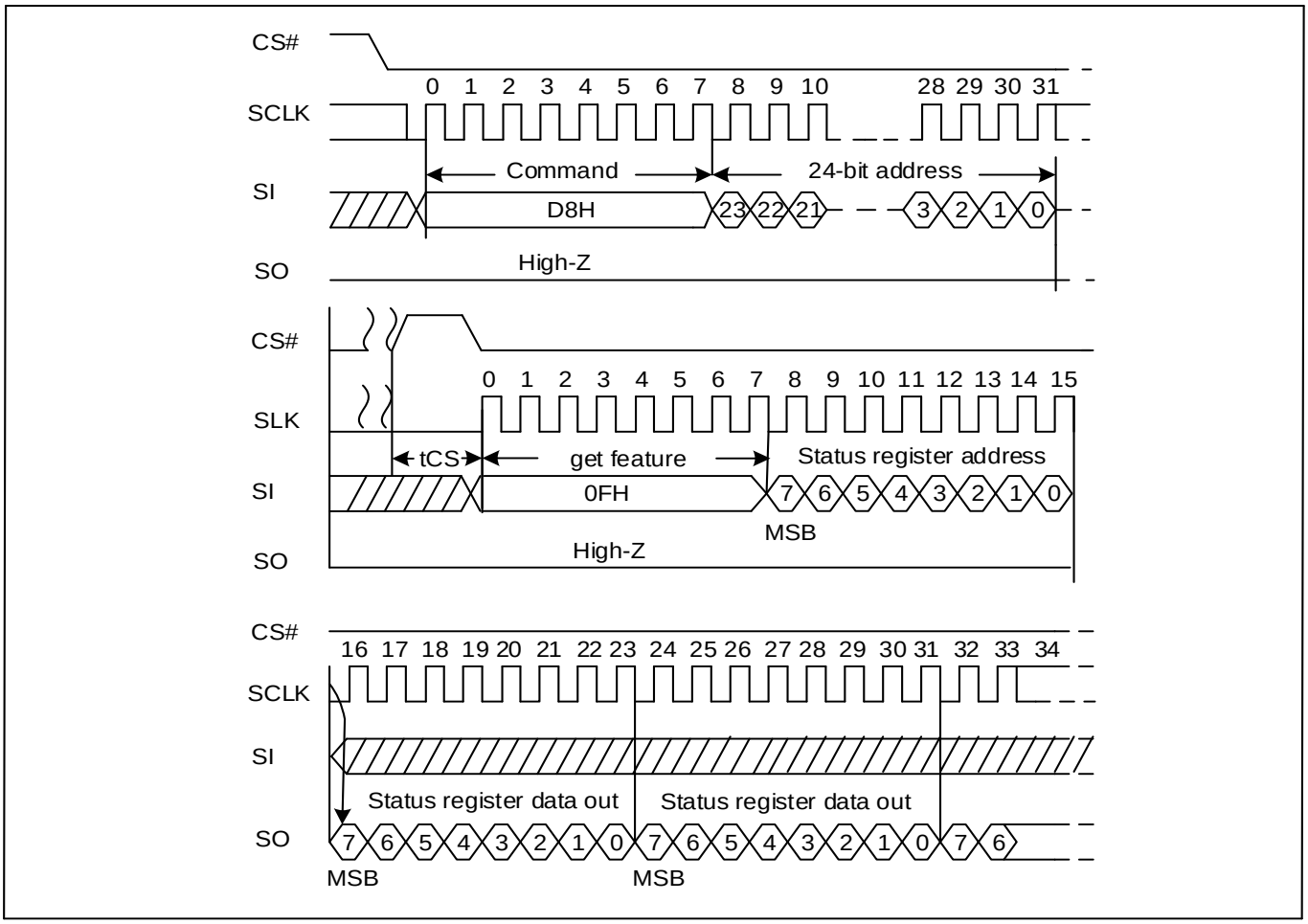
10.1 Block Erase (D8H)

The BLOCK ERASE (D8H) command is used to erase at the block level. The blocks are organized as 64 pages per block, The BLOCK ERASE command (D8H) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06H (WRITE ENBALE command)
- D8H (BLOCK ERASE command)
- 0FH (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8H) command. This command requires a 24-bit address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tBERS time during the BLOCK ERASE operation. The GET FEATURES (0FH) command can be used to monitor the status of the operation.

Figure 10. Block Erase Sequence Diagram

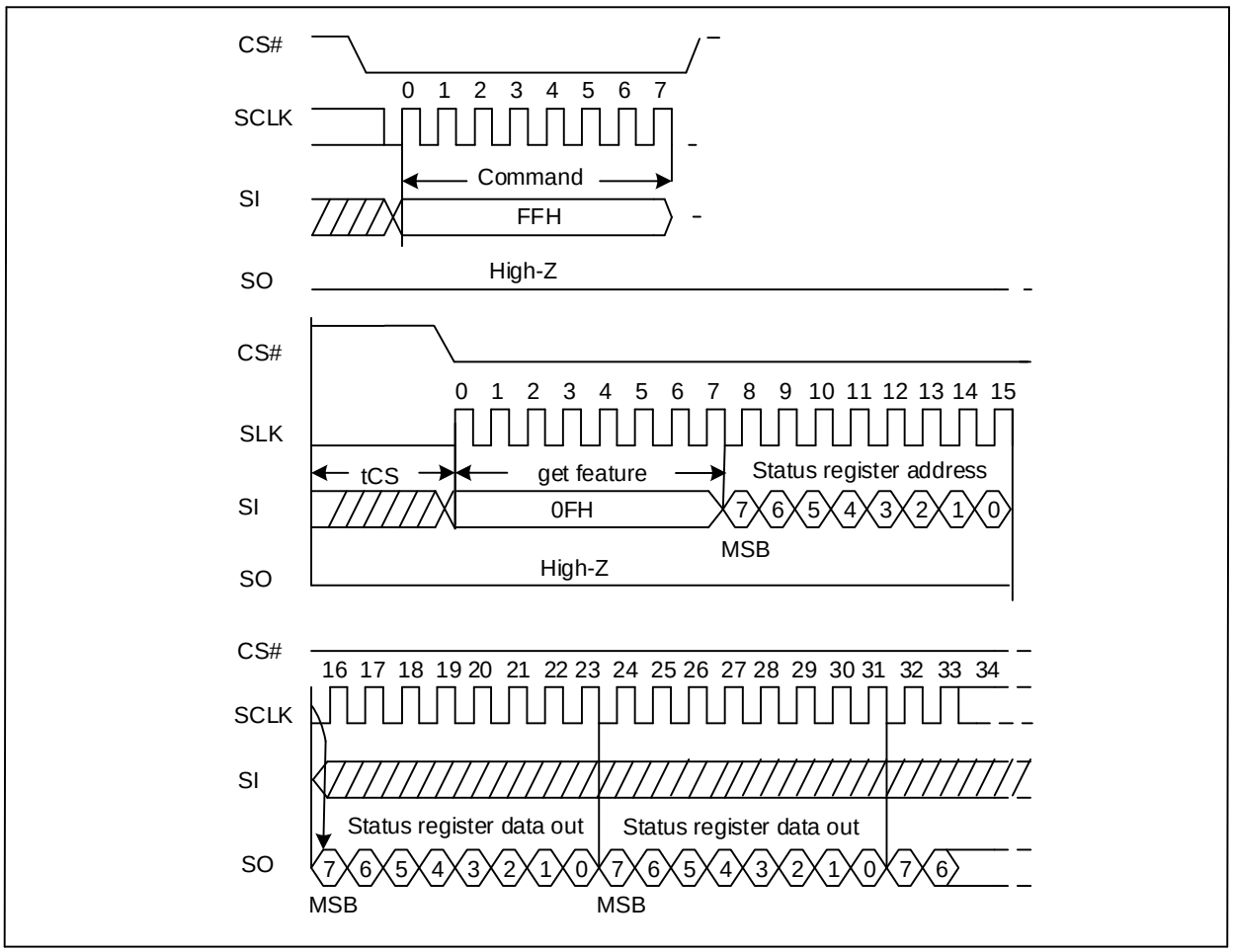


11 RESET OPERATIONS

11.1 Soft Reset (FFH)

The RESET (FFH) command stops all operations and status. For example, in case of a program or erase or read operation, the reset command can make the device enter the wait state.

Figure 11. Reset Sequence Diagram



Note: The Register bit value after soft reset refers to Table 12-2.Register bit Descriptions.

12 FEATURE OPERATIONS

12.1 Get Features (0FH) and Set Features (1FH)

The GET FEATURES (0FH) and SET FEATURES (1FH) commands are used to monitor the device status and alter the device behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP can be enabled or disabled by setting specific feature bits (shown in the following table). The status register is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06H) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFH) command is issued.

Table12_1. Features Settings

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	Reserved	Reserved	Reserved	QE
Status	C0H	Reserved	ECCS2	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Feature	D0H	Reserved	DS_IO[1]	DS_IO[0]	Reserved	Reserved	Reserved	Reserved	Reserved

Note:

If BRWD is enabled and WP# is LOW, then the block lock register cannot be changed.

If QE is enabled, the quad IO operations can be executed.

All the reserved bits must be held low when the feature is set.

These registers A0H/B0H/D0H are write/read type, and Registers C0H are read only.

The OTP_PRT is non-volatile, others bits are volatile.

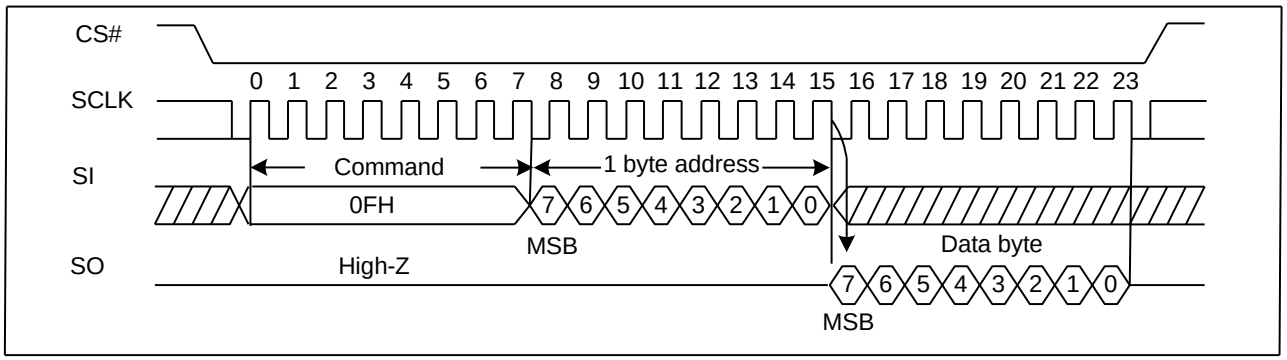
The Register Bit default value after power-up refers to Table12-2.Register Bit Descriptions.

Table12-2. Register Bit Descriptions

Bit	Bit Name	After Power up	After Reset command (FFH)	Description
BRWD	Block register write disable	0	No Change	Which is used combined with WP#, If BRWD is high enabled and WP# is LOW, then the Protection register cannot be changed.
BP2 BP1 BP0 INV CMP	Block Protection bits	1 1 1 0 0	No Change	Used combination, refer to chapter Block Protection
OTP_PRT OTP_EN	OTP Region bits	0 0 Before OTP set	No Change	Used combination, refer to chapter OTP Region
ECC_EN	ECC Enable Latch	1	No Change	The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled by default when device powered on, so the default READ and PROGRAM commands operate with internal ECC in the “active” state when ECC enable.
QE	The Quad Enable bit	0	No Change	This bit indicates that whether the quad IO operations can be executed. If QE is set to 1, the quad IO operations can be executed.
ECCS0 ECCS1 ECCS2	ECC Status	Page 0 Status	0 0 0	ECCS provides ECC status as the following table. ECCS is set to 000b either following a RESET, or at the beginning of the READ. They are then updated after the device completes a valid READ operation. ECCS is invalid if internal ECC is disabled (via a SET FEATURES command to reset ECC_EN to 0). After power-on RESET, ECC status is set to reflect the contents of block 0, page 0.
P_FAIL	Program Fail	0	0	This bit indicates that a program failure has occurred (P_FAIL =1). It will also be set if the user attempts to program a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_FAIL = 0).
E_FAIL	Erase Fail	0	0	This bit indicates that an erase failure has occurred (E_FAIL =1). It will also be set if the user attempts to erase a locked region. This bit is cleared (E_FAIL = 0) at the start of the BLOCK ERASE command sequence or the RESET command.

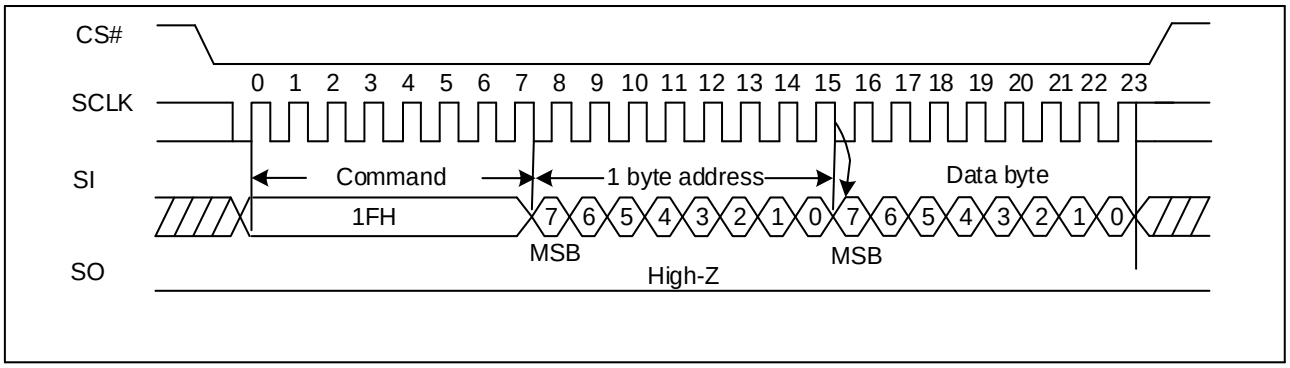
WEL	Write Enable Latch	0	0	This bit indicates the current status of the write enable latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	0	0	This bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.
DS_IO[0] DS_IO[1]	Driven Strength register	0 0	No Change	IO driver strength setting. Default is 00b.

Figure 12_1. Get Features Sequence Diagram



Note: The output would be updated by real-time, until CS# is driven high.

Figure 12_2. Set Features Sequence Diagram



12.2 Status Register and Driver Register

The NAND Flash device has an 8-bit status register that software can read during the device operation for operation state query. The status register can be read by issuing the GET FEATURES (0FH)command, followed by the feature address C0h (see FEATURE OPERATION). The Output Driver Register can be set and read by issuing the SET FEATURE (0FH) and GET FEATURE command followed by the feature address D0h (see FEATURE OPERATION)..

Table12_3. ECC Status

ECCS2	ECCS1	ECCS0	Description
0	0	0	No bit errors were detected during the previous read algorithm.
0	0	1	Bit errors(≤3) were detected and corrected.
0	1	0	Bit errors(=4) were detected and corrected.
0	1	1	Bit errors(=5) were detected and corrected.
1	0	0	Bit errors(=6) were detected and corrected.
1	0	1	Bit errors(=7) were detected and corrected.
1	1	0	Bit errors(=8) were detected and corrected.
1	1	1	Bit errors>8, error exceeded. And cannot be corrected.

Table12_4. Driver Register Bits Descriptions

DS_S1	DS_S0	Driver Strength
0	0	50%
0	1	25%
1	0	75%
1	1	100%

12.3 OTP Region

The serial device offers a protected, One-Time Programmable NAND Flash memory area. 4 full pages are available on the device. Customers can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0. To access the OTP feature, the user must set feature bits OTP_EN/OTP_PRT by SET FEATURES command. When the OTP is ready for access, only pages 00h–03H can be programmed in sequential order by PROGRAM LOAD (02H) and PROGRAM EXECUTE(10H) commands (when not yet protected), and read out by PAGE READ (13H) command and output data by READ from CACHE(03H/0BH/3BH/6BH).

Whether ECC is enabled or disabled, data written in the OTP area is ECC protected.

Table12_5. OTP States

OTP_PRT	OTP_EN	State
x	0	Normal operation
0	1	Access OTP region, read and program data.
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue PROGRAM EXECUTE (10H) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data.

Note: The OTP space cannot be erased and after it has been protected, it cannot be programmed again, please use this function carefully.

Access to OTP data

- Issue the SET FEATURES command (1FH)
- Set feature bit OTP_EN
- Issue the PAGE PROGRAM (only when OTP_PRT is 0) or PAGE READ command

Protect OTP region

Only when the following steps are completed, the OTP_PRT will be set and users can get this feature out with 0FH command.

- Issue the SET FEATURES command (1FH)
- Set feature bit OTP_EN and OTP_PRT
- 06H (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10H) command.

Note：If user programs the OTP region data after OTP_PRT is 1, user needs to issue the Soft Reset (FFh) before exiting OTP mode.

12.4 Block Protection

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the “locked” state, i.e., feature bits BP0, BP1and BP2 are set to 1, INV, CMP and BRWD are set to 0. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued to alter the state of protection feature bits. When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set. Also, when a PROGRAM/ERASE command is issued to a locked block, status bit OIP remains 0. When an ERASE command is issued to a locked block, the erase failure, status bit E_FAIL set to 1. When a PROGRAM command is issued to a locked block, program failure, status bit P_FAIL set to 1.

To enable the Write Protection (WP#), the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

Table12_6. Block Lock Register Block Protect Bits

CMP	INV	BP2	BP1	BP0	Protect Row Address	Protect Rows
					4Gb	
x	x	0	0	0	NONE	None—all unlocked
0	0	0	0	1	1F800h ~ 1FFFFh	Upper 1/64 locked
0	0	0	1	0	1F000h ~ 1FFFFh	Upper 1/32 locked
0	0	0	1	1	1E000h ~ 1FFFFh	Upper 1/16 locked
0	0	1	0	0	1C000h ~ 1FFFFh	Upper 1/8 locked
0	0	1	0	1	18000h ~ 1FFFFh	Upper 1/4 locked
0	0	1	1	0	10000h ~ 1FFFFh	Upper 1/2 locked
x	x	1	1	1	0000h ~ 1FFFFh	All locked (default)
0	1	0	0	1	0000h ~7FFh	Lower 1/64 locked
0	1	0	1	0	0000h ~FFFh	Lower 1/32 locked
0	1	0	1	1	0000h ~ 1FFFh	Lower 1/16 locked
0	1	1	0	0	0000h ~ 3FFFh	Lower 1/8 locked
0	1	1	0	1	0000h ~ 7FFFh	Lower 1/4 locked
0	1	1	1	0	0000h ~ FFFFh	Lower 1/2 locked
1	0	0	0	1	0000h ~ 1F7FFh	Lower 63/64 locked
1	0	0	1	0	0000h ~ 1EFFFh	Lower31/32 locked
1	0	0	1	1	0000h ~ 1DFFFh	Lower 15/16 locked
1	0	1	0	0	0000h ~ 1BFFFh	Lower7/8 locked
1	0	1	0	1	0000h ~ 17FFFh	Lower3/4 locked
1	0	1	1	0	0000h ~ 003Fh	Block0
1	1	0	0	1	0800h ~ 1FFFFh	Upper 63/64 locked
1	1	0	1	0	1000h ~ 1FFFFh	Upper31/32 locked
1	1	0	1	1	2000h ~ 1FFFFh	Upper 15/16 locked
1	1	1	0	0	4000h ~ 1FFFFh	Upper7/8 locked
1	1	1	0	1	8000h ~ 1FFFFh	Upper3/4 locked
1	1	1	1	0	0000h ~ 003Fh	Block0

When WP# is not LOW, user can issue bellows commands to alter the protection states as want.

- Issue SET FEATURES register write (1FH)
- Issue the feature bit address (A0h) and the feature bits combination as the table.

13 ADVANCED FEATURES

13.1 Assistant Bad Block Management

As a NAND Flash, the device may have blocks that are invalid when shipped from the factory, and a minimum number of valid blocks (N_{VB}) of the total available blocks are specified. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below N_{VB} during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms, which ensure data integrity. Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by programming the Bad Block Mark (00h) to the first spare area location in each bad block. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFH data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

To simplify the system requirement and guard the data integration, GigaDevice SPI NAND provides assistant Management options as below.

Table13_1. Bad Block Mark information

Description	Density	Requirement
Minimum number of valid blocks (N_{VB})	4G	2008
Total available blocks per die	4G	2048
First spare area location		Byte 4096
Bad-block mark		00h(use non FFH to check)

13.2 Internal ECC

The serial device offers data corruption protection by offering optional internal ECC.READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the “active” state.

To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURES command (1FH) to set the feature bit ECC_EN:
  1. To enable ECC, Set ECC_EN to 1.
  2. To disable ECC, Clear ECC_EN to 0.

During a PROGRAM operation, the device calculates an ECC code on the 4k page in the cache register, before the page is written to the NAND Flash array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If error bits are detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

The ECC protection format as follow:

- All data in main area and spare areas data are protected.

Any data wrote to the ECC parity data area are ignored when ECC enabled.

Table13-2. The Distribution of ECC Segment and Spare Area in a Page

Main Area(4KB)								Spare Area(256B)								
User data(4KB)								User meta data(128B)								ECC Parity Data(128B)
Main0	Main1	Main2	Main3	Main4	Main5	Main6	Main7	Spare0	Spare1	Spare2	Spare3	Spare4	Spare5	Spare6	Spare7	ECC Area
(512B)	(512B)	(512B)	(512B)	(512B)	(512B)	(512B)	(512B)	(16B)	(16B)	(16B)	(16B)	(16B)	(16B)	(16B)	(16B)	(128B)

Table13_3. ECC Protection and Spare Area

Min Byte Address	Max Byte Address	ECC Protected	Area	Description
000H	1FFH	Yes	Main 0	User data 0
200H	3FFH	Yes	Main 1	User data 1
400H	5FFH	Yes	Main 2	User data 2
600H	7FFH	Yes	Main 3	User data 3
800H	9FFH	Yes	Main 4	User data 4
A00H	BFFH	Yes	Main 5	User data 5
C00H	DFFH	Yes	Main 6	User data 6
E00H	FFFH	Yes	Main 7	User data 7
1000H	100FH	Yes	Spare 0	User meta data 0(1)
1010H	101FH	Yes	Spare1	User meta data 1
1020H	102FH	Yes	Spare2	User meta data 2
1030H	103FH	Yes	Spare3	User meta data 3
1040H	104FH	Yes	Spare4	User meta data 4
1050H	105FH	Yes	Spare5	User meta data 5
1060H	106FH	Yes	Spare6	User meta data 6
1070H	107FH	Yes	Spare7	User meta data 7
1080H	10FFH	Yes	Spare Area	Internal ECC parity data

Note

1: 1000H is reserved for initial bad block mark, and please check the initial bad block mark with internal ECC off.

2. When Internal ECC is enabled, user cannot program the Address 1080H~10FFH but user can read the Address 1080H~10FFH.

3 .When Internal ECC is disabled, the whole page area is open for user. And we recommend the user to provide external ECC protection.

14 POWER ON TIMING

Figure 14. Power on Timing Sequence

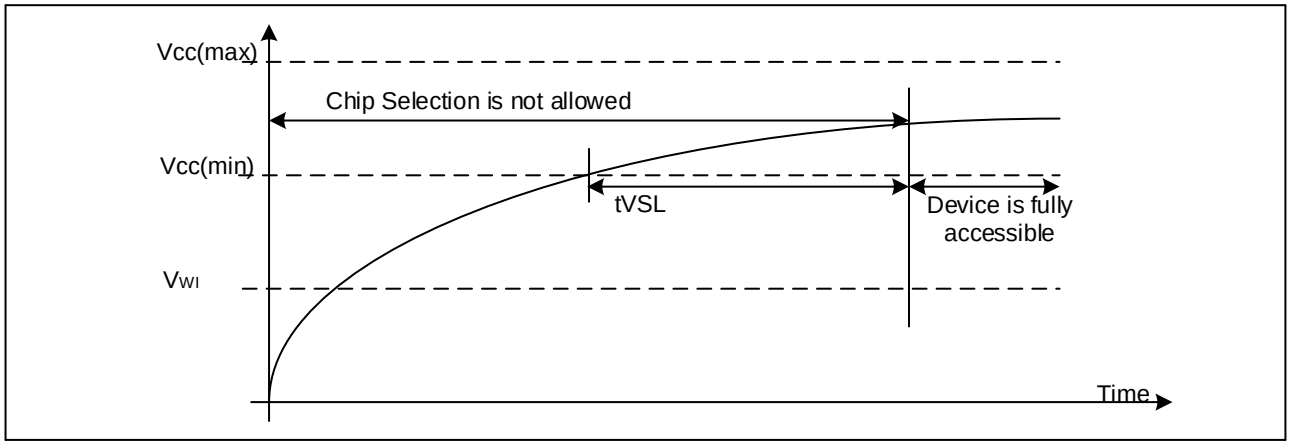


Table14. Power-On Timing and Write Inhibit Threshold for 1.8V/3.3V

Symbol	Parameter		Min	Max	Unit
tVSL	VCC(min) To CS# Low		2		ms
VWI	Write Inhibit Voltage	1.8V		1.7	V
		3.3V		2.5	

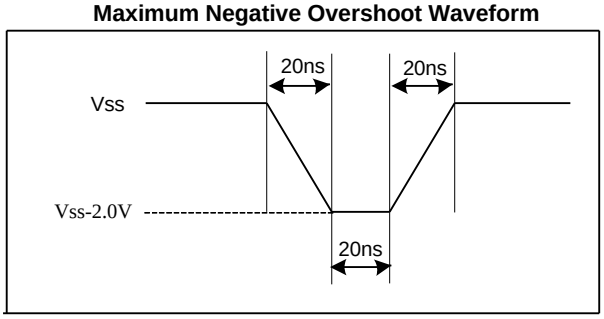
15 ABSOLUTE MAXIMUM RATINGS

Table15. Absolute Maximum Ratings

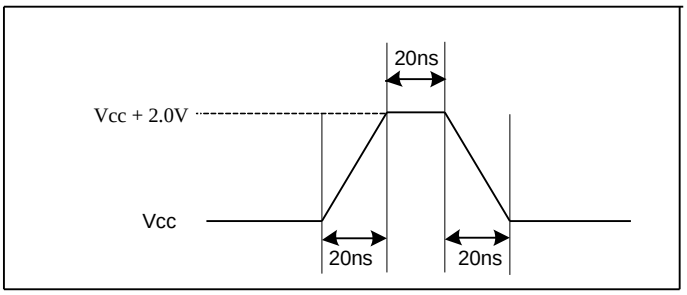
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Applied Input/Output Voltage	-0.6 to VCC+0.4	V
VCC(3.3V)	-0.6 to 4.0	V
VCC(1.8V)	-0.6 to 2.5	V

Figure15-1. Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform



16 Operating Ranges

Table16. Operating Ranges

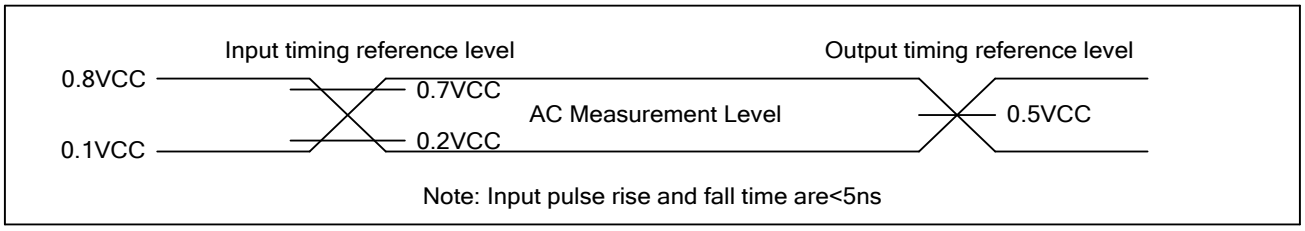
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
T_A	Ambient Operating Temperature	-40		85	℃	Industrial
VCC(1.8V)	Supply Voltage for 1.8V series	1.7	1.8	2.0	V	
VCC(3.3V)	Supply Voltage for 3.3V series	2.7	3.3	3.6	V	

17 CAPACITANCE MEASUREMENT CONDITIONS

Table17. Capacitance Measurement Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure17. Input Test Waveform and Measurement Level



18 DC CHARACTERISTIC

Table18. DC Characteristic

(T= -40℃~85℃, VCC=1.7~2.0V/2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±10	μA
I_{LO}	Output Leakage Current				±10	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS			90	μA
I_{CC2}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 120MHz, Q=Open(*1,*2,*4 I/O)			40	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)			30	mA
I_{CC3}	Operation Current (PP)	CS#=VCC			40	mA
I_{CC4}	Operation Current (BE)	CS#=VCC			40	mA
V_{IL}	Input Low Voltage				0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC			V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

19 AC CHARACTERISTICS

Table19. AC Characteristic

(T= -40℃~85℃, VCC=1.7~2.0V/2.7~3.6V, C_L=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
F_C	Serial Clock Frequency For: all command	DC.		120	MHz
tCH	Serial Clock High Time	4			ns
tCL	Serial Clock Low Time	4			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# Not Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL/tCS	CS# High Time	20			ns
tSHQZ	Output Disable Time			20	ns
tCLQX	Output Hold Time	2			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	Hold# Low Setup Time (relative to Clock)	5			ns
tHHCH	Hold# High Setup Time (relative to Clock)	5			ns
tCHHL	Hold# High Hold Time (relative to Clock)	5			ns
tCHHH	Hold# Low Hold Time (relative to Clock)	5			ns
tHLQZ	Hold# Low To High-Z Output			15	ns
tHHQX	Hold# HighTo Low-Z Output			15	ns
tCLQV	Clock Low To Output Valid			8	ns
tWHSL	WP# Setup Time Before CS# Low	20			ns
tSHWL	WP# Hold Time After CS# High	100			ns

20 PERFORMANCE TIMING

Table20. Performance Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tRST	CS# High To Next Command After Reset(FFh)			500	us
tRD	Read From Array			120	us
tPROG	Page Programming Time		480	700	us
tBERS	Block Erase Time		3	10	ms

Figure20_1. Serial Input Timing

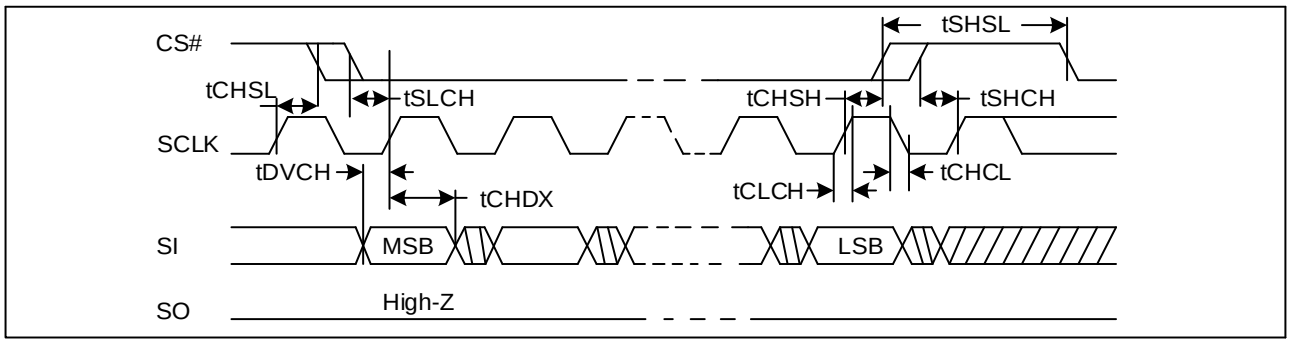


Figure20_2. Output Timing

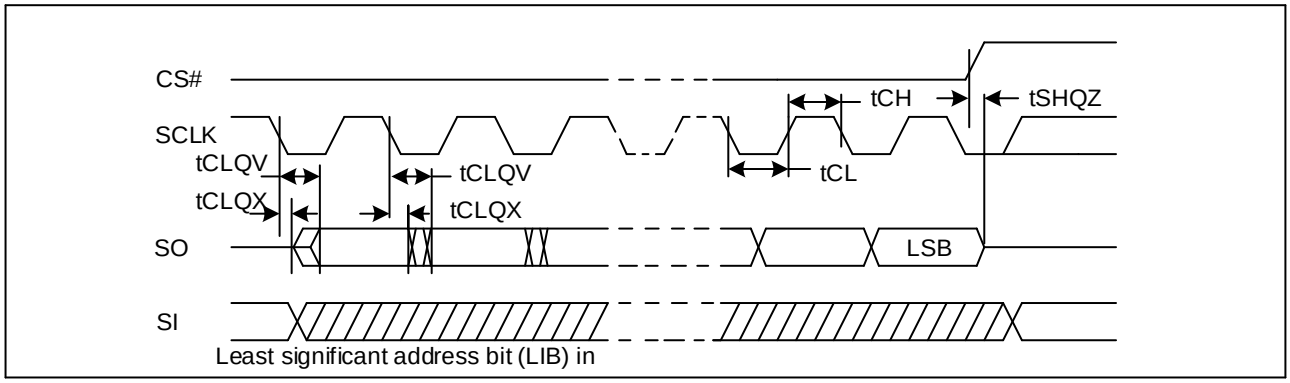


Figure20_3. Hold Timing

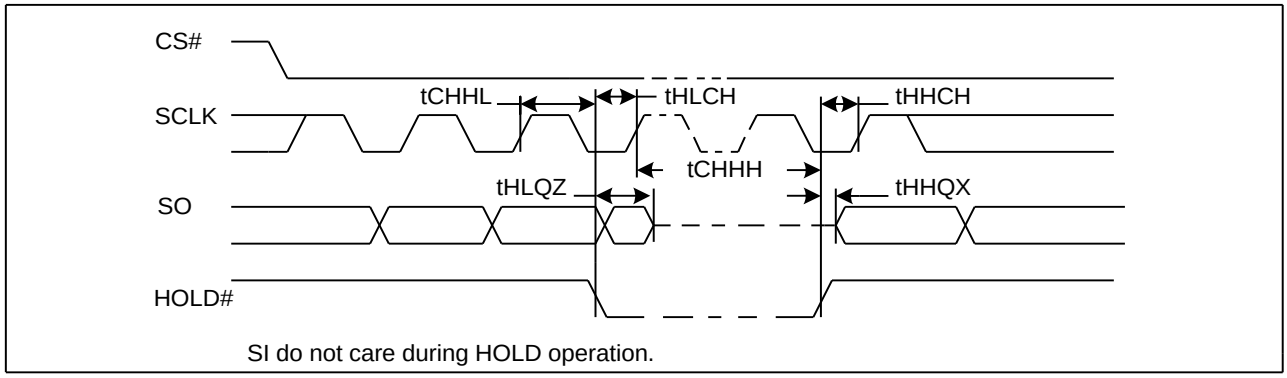
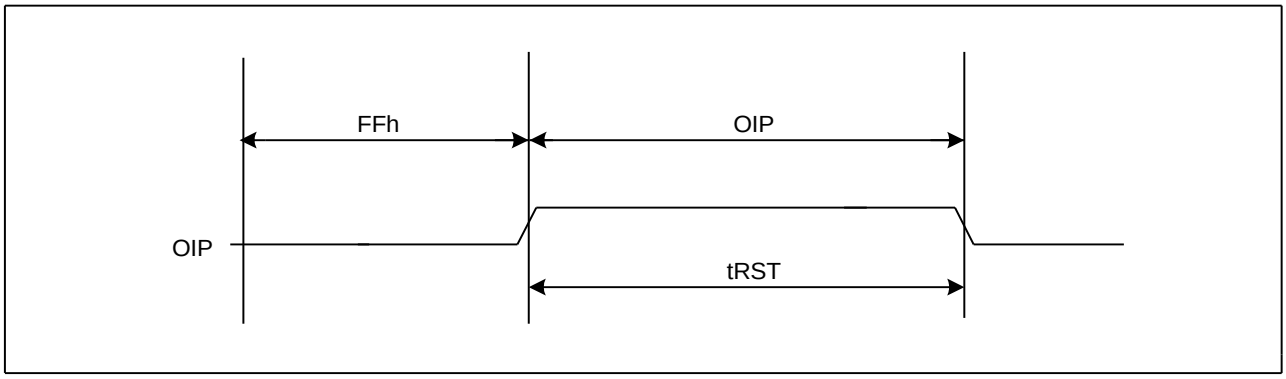


Figure20_4. Reset Timing



Note: The maximum Trst depends on different operations.

Idle: maximum Trst = 5us;

Read: maximum Trst = 10us;

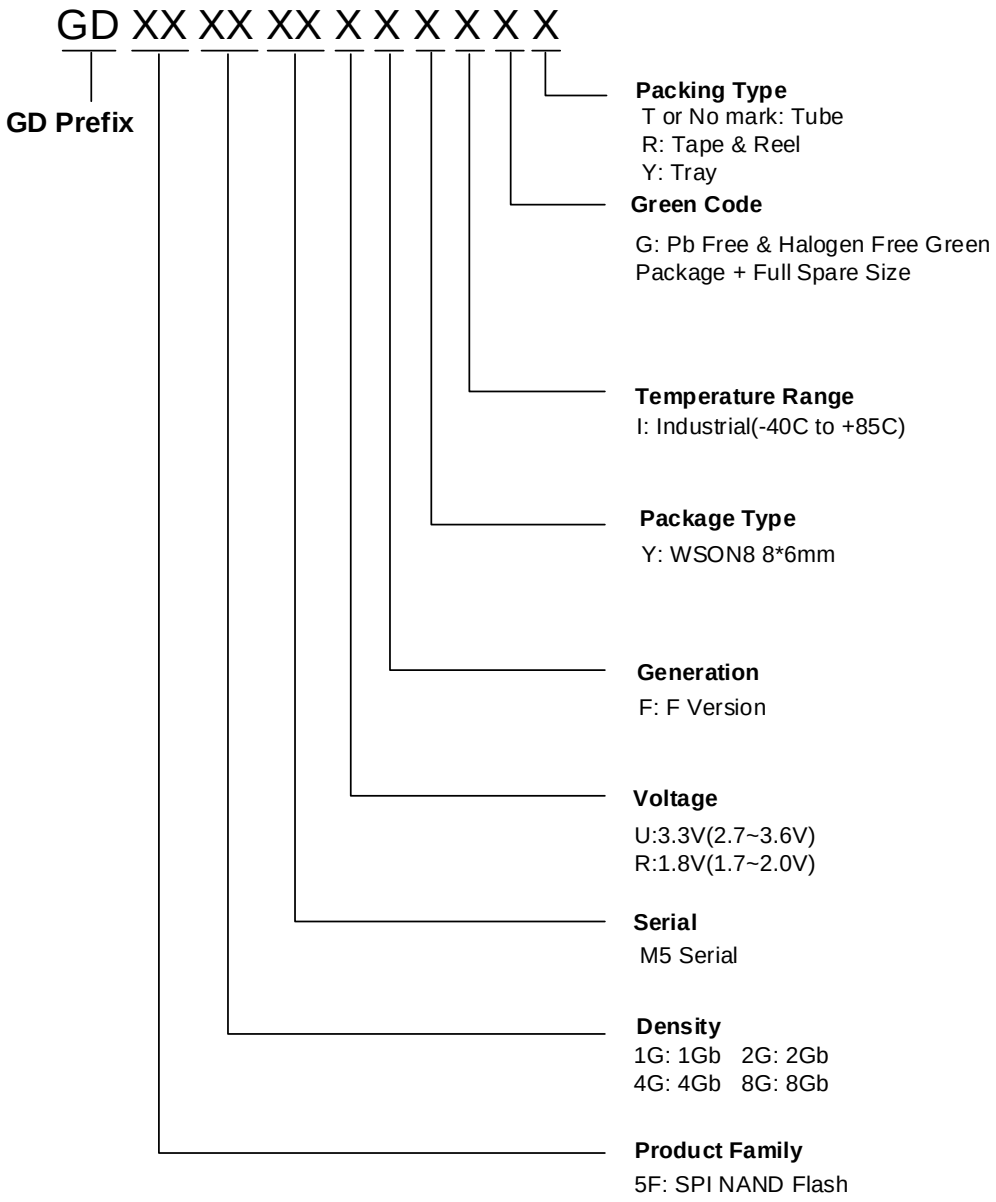
Program: maximum Trst = 20us;

Erase: maximum Trst = 500us;

21 ORDERING INFORMATION

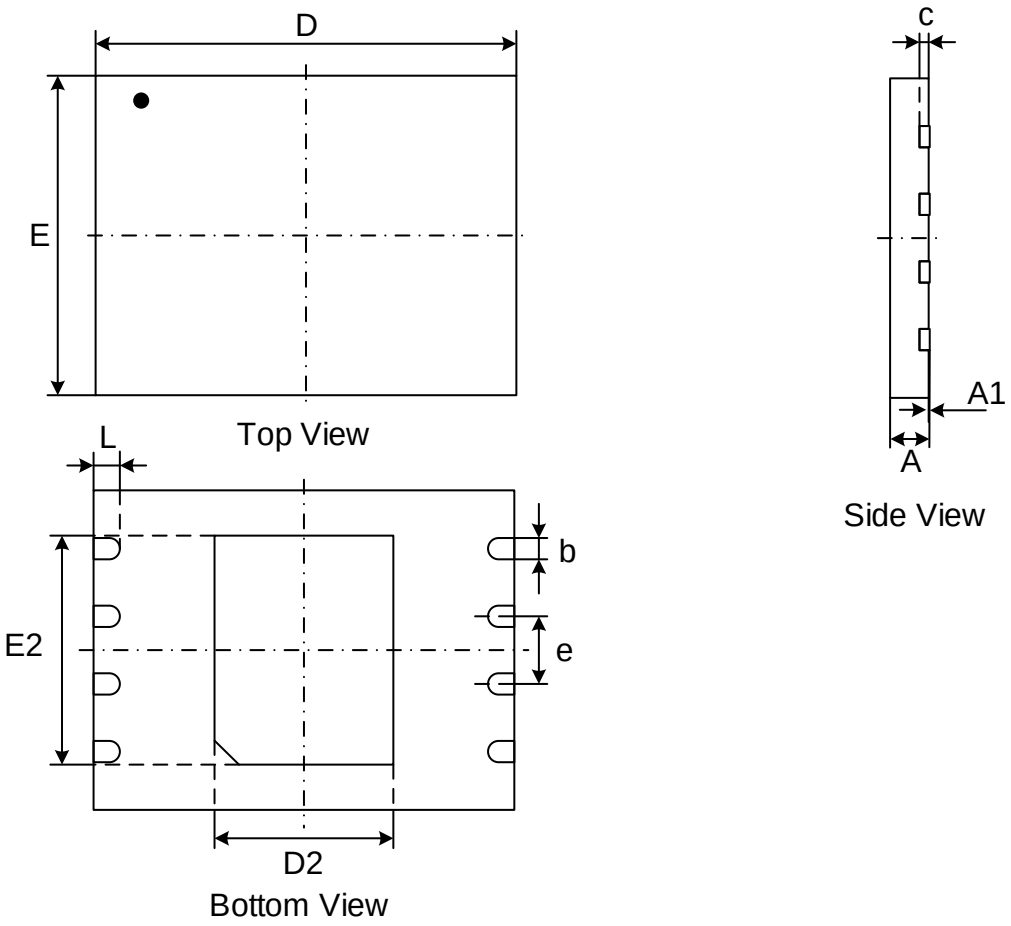
Table21.Product List

Product Number	Density	Voltage	Package Type	Temperature
GD5F4GM5RFYIG	4Gbit	1.7V to 2.0V	WSON8(8*6mm)	-40℃ to 85℃
GD5F4GM5UFYIG		2.7V to 3.6V	WSON8(8*6mm)	-40℃ to 85℃



22 PACKAGE INFORMATION

Figure22_1. WSON8 (8*6mm)



Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55
Inch	Min	0.028	0	0.007	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom	0.030	0.001	0.008	0.016	0.315	0.134	0.236	0.169		0.020
	Max	0.032	0.002	0.010	0.018	0.319	0.138	0.240	0.173		0.022

23 REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial Release		2020-09-01

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