HH Zealcore SPI 2G

Serial Peripheral Interface (SPI)
NAND Flash

Parts No.	Density	Voltage	Package	MID	DID	Page Size	Pages/block
HF2GQ4UDACAE	2Gb/256MB	3.3V	WSON8	C9	22	2K	64
HF2GQ4UDDCAE	2Gb/256MB	3.3V	TFBGA24	C9	22	2K	64

Revision History

Publication Version:	V1.4 03/20/2018
Note:	Add Package TFBGA24
Publication Version:	V1.3 09/27/2017
Note:	Modify supply voltage minimum 2.9V
Publication Version:	V1.2 08/29/2017
Note:	Modify Default: Sleep mode turn off
Publication Version:	V1.1 05/31/2017
Note:	Divide into 3.3v (only)
Publication Version:	V1.0 03/20/2017
Note:	First Release

SPI (Serial Peripheral Interface) NAND Flash Memory 2Gb

Features

☆ Standard Dual and Quad SPI
- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
- Quad SPI: SCLK, CS# ,SIO0, SIO1, SIO2, SIO3

☆ Advanced Feature for SLC NAND Flash
- ECC 4 bit/512B
- Read/Write access frequency option
- Internal data move page with ECC
- Bad-Block mapping management is not needed
- 2K+64 byte for cache read and program

☆ Flash Features
- Block Size
  # (Page size) x (64 page/block)
- Page Size
  # 2048 + 64 bytes
- SPI Capacity
  # 2Gb : 2048 blocks
- The first block to 2000th block are good for 2Gb

☆ Low Power Consumption
- 40mA maximum power dissipation
- 70uA maximum standby current @ sleep mode

☆ SPI Max. Clock Frequency
- 80MHz @ 3.3V

☆ SPI power supply voltage
- Full voltage range for 3.3V : 2.9 to 3.6V

☆ Software/Hardware write protection
- Write protection all/portion blocks with software
- Enable/Disable protection with WP#/SIO2 pin

☆ Security Features
- 8K bytes OTP region

Note : Sleep mode is turn off in default. If you need power-down mode, please ask for us.

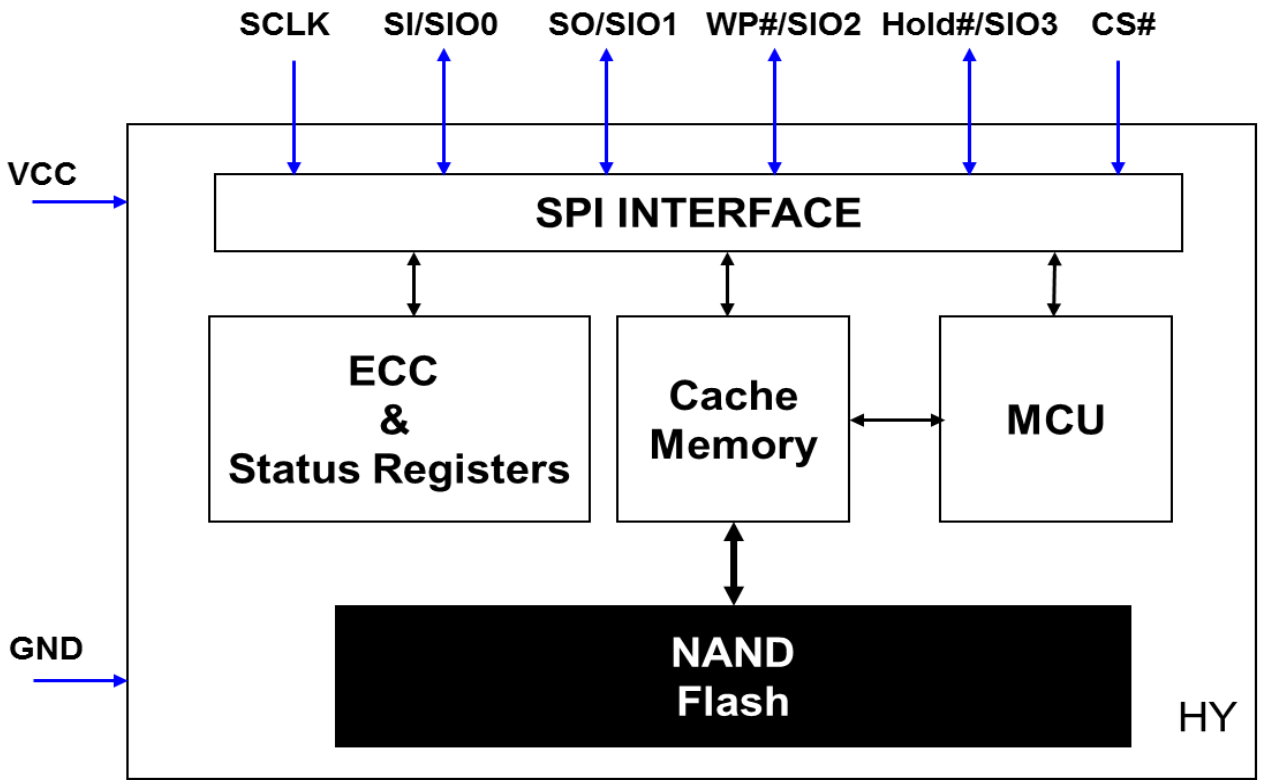
General Description

SPI (Serial Peripheral Interface) NAND Flash provides a low cost and low pin count solution to alternate SPI-NOR in high density non-volatile memory storage solution for embedded systems.

SPI NAND Flash is an SLC NAND Flash memory device based on the standard parallel NAND Flash. The serial electrical interface follows the industry-standard serial peripheral interface. The command sets is similar to the SPI-NOR command sets but with some modifications to handle NAND specific functions and new features are added to extend applications. The SPI NAND flash device has total 8 pin count, including six signal lines plus VCC and GND.

Each block of the serial NAND Flash device is subdivided into 64 programmable pages. Each page consists of a data storage region and a spare area. The data storage region is used to storage data user programmed and the spare area is typically used for memory management and error correction functions.

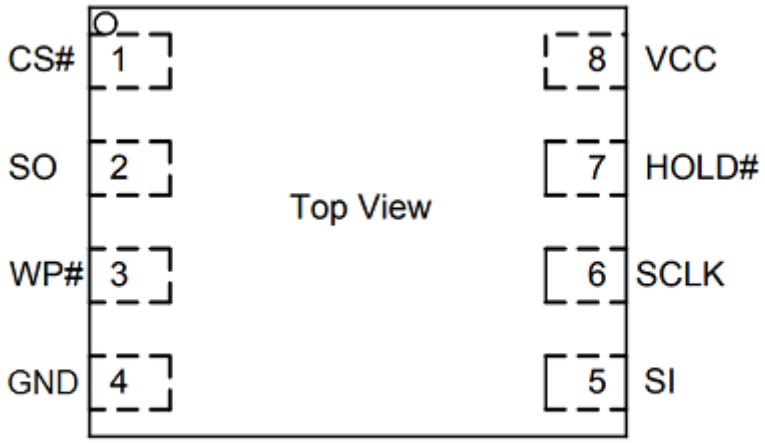
Functional Block Diagram



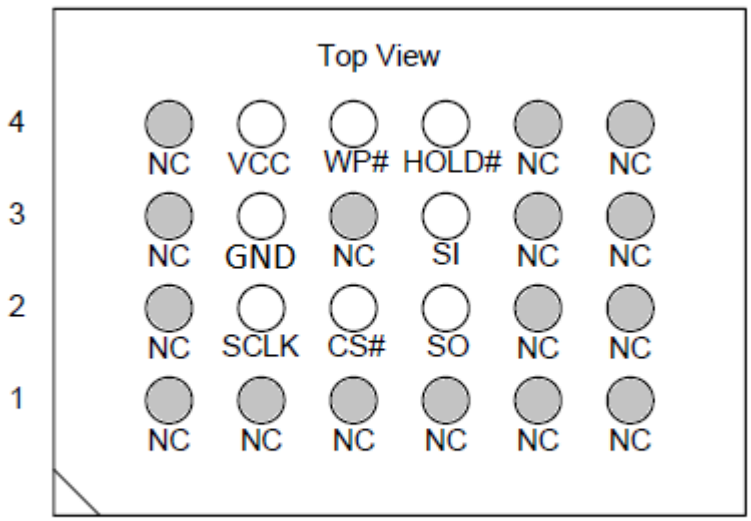
Pin Description

Pin Name	Type	Description
SCLK	In	Serial Clock
SI/SIO0	I/O	Serial Data Input / Serial Data I/O0
SO/SIO1	I/O	Serial Data Output / Serial Data I/O1
WP#/SIO2	I/O	Write Protect / Serial Data I/O2
Hold#/SIO3	I/O	Hold / Serial Data I/O3
CS#	In	Chip Select
VCC	Supply	Power Supply
GND	Ground	Ground

Connection Diagram (Included SPI controller and NAND Flash)



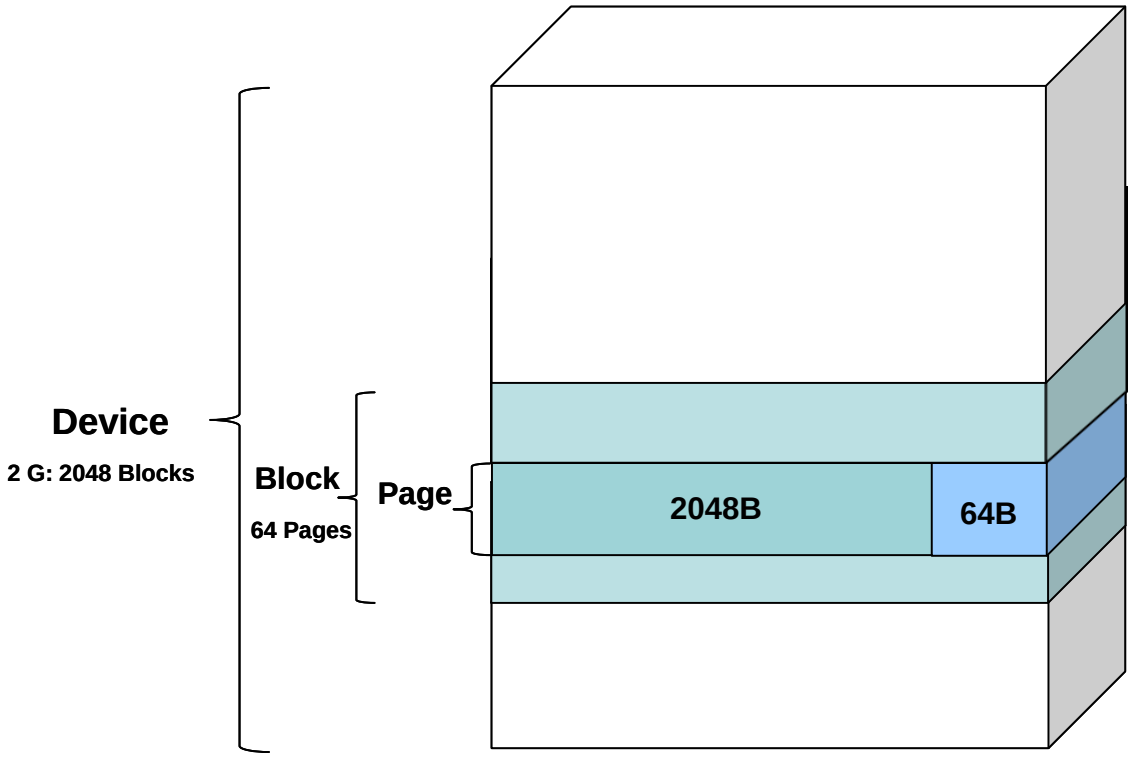
WSON-8



24-BALL TFBGA

Array Organization

Device	Number of Blocks	Number of Pages	Page Size	Device Size
2G	2048	64	2K+64B	256MB+8MB

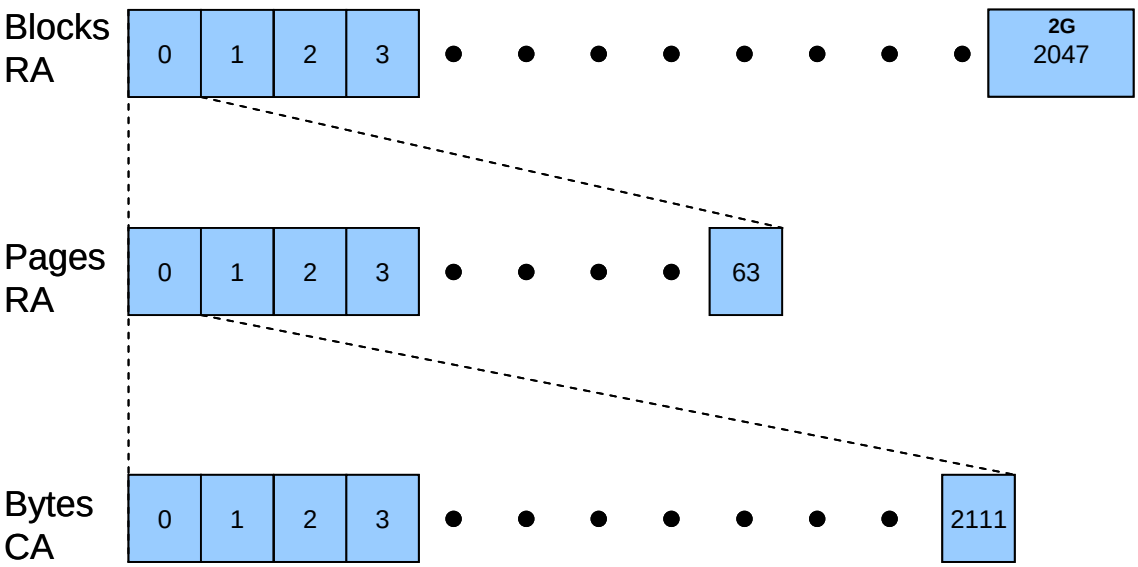


1 page (program unit) = (2K+64) bytes

1 block (Erase unit) = (2K+64)*64 pages = (128K+4K) bytes

2 G device = (128K+4K)*2048 blocks = (256MB+8MB)

MEMORY MAPPING



Note:

1. RA: Row Address. The RA can to index and select the block.

   RA[5:0]: for Page Range 0~63.

   RA[16:6] : for 2G, have 0~2047 blocks range.

2. CA: Column Address. The CA[11:0] can only access 0~2111 bytes, include 2K(2048)bytes and 64Byte *OOB.

   *OOB : Each page of a NAND flash has an “out of band” (OOB) area to hold Error Correcting Code (ECC) and other metadata.

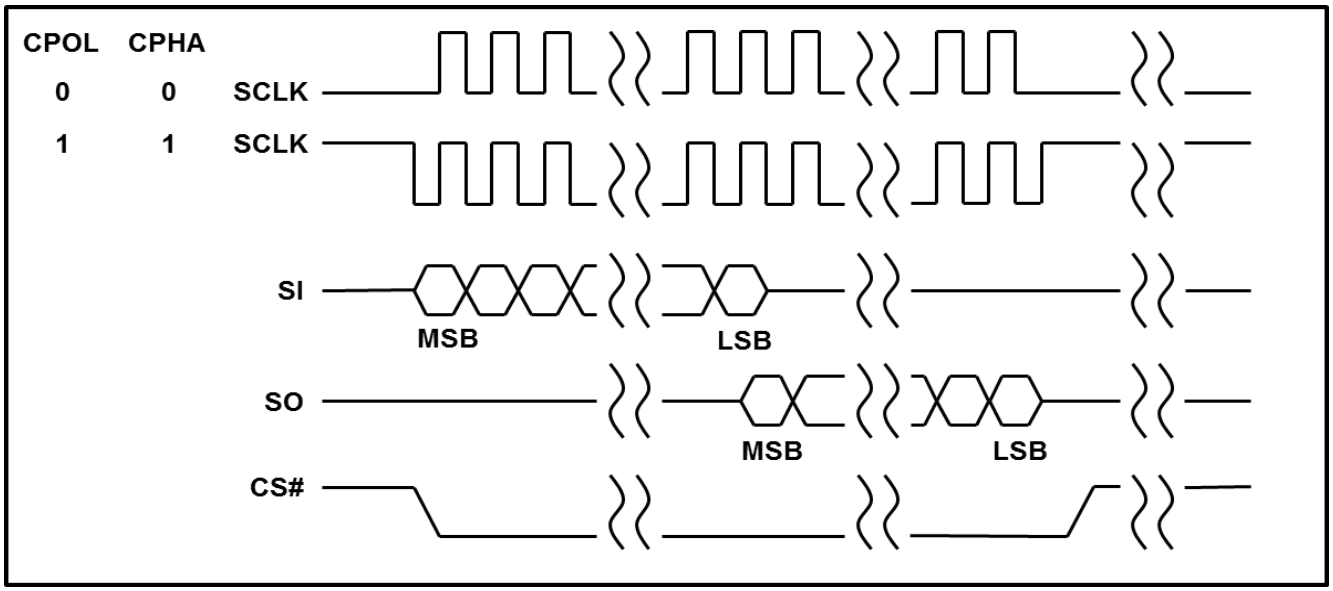
Device Operation

SPI Mode

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCLK and output data is available on the falling edge of SCLK for both mode 0 and mode 3. The timing diagrams shown in this data sheet are mode 0.



SCLK	SCLK provides interface timing for SPI NAND. Address, data and commands are latched on the rising edge of SCLK. Data is placed on SO at the falling edge of SCLK.
CS#	When CS# = 0, the device is placed in active mode. When CS# = 1, the device is placed in inactive mode and SO is High-Z.

Standard SPI:

Standard serial peripheral interface on four signals bus: System Clock (SCLK), Chip Select (CS#), Serial Data In (SI) and Serial Data Out (SO).

Dual SPI:

SPI NAND supports dual SPI operation with x2 and dual IO commands. These commands allow data to be transferred to or from SPI NAND at two times of rates of Standard SPI operation. The SI and SO become bi-directional I/O pins : SIO0 and SIO1.

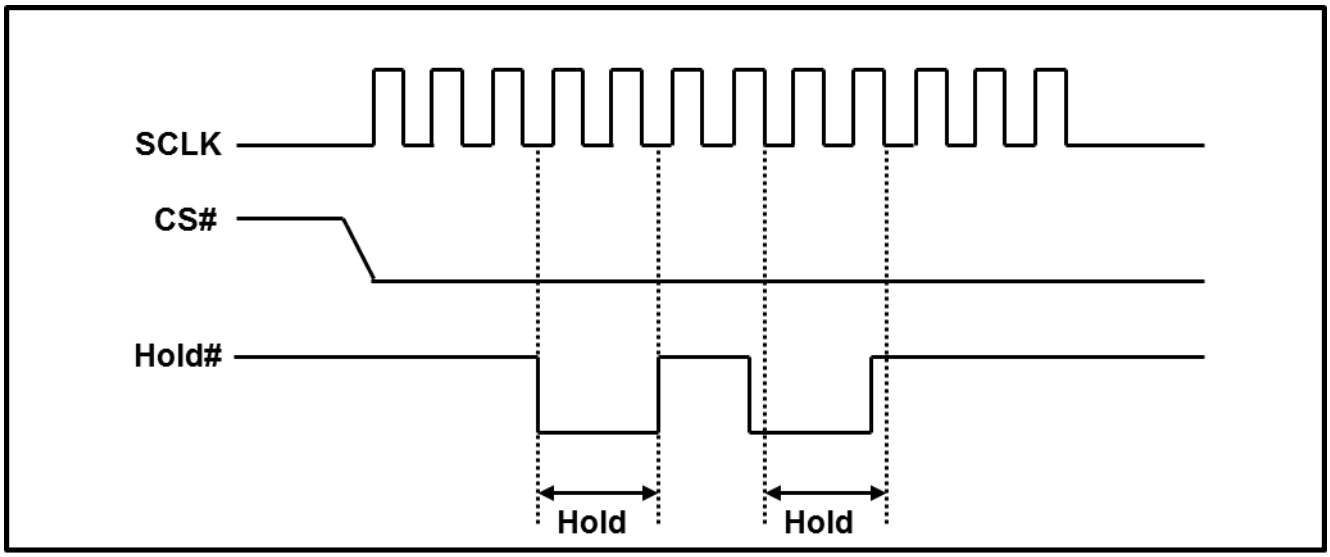
Quad SPI:

SPI NAND supports the x4 and Quad commands operation. These commands allow data to be transferred to or from SPI NAND at four times of rates of Standard SPI operation. The SI and SO become bi-directional I/O pins: SIO0 and SIO1, the WP# and HOLD# pins become SIO2 and SIO3.

Hold Mode:

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming or erasing in progress.

Hold Condition Diagram



HOLD	Hold mode starts at the falling edge of HOLD# provided SCLK is also LOW. If SCLK is HIGH when HOLD# goes LOW, hold mode begins after the next falling edge of SCLK.

Write Protection Mode:

Write protect (WP#) provides hardware protection mode. The WP# prevents the block lock bits (BP0, BP1, and BP2) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

SPI NAND Flash Command Set

Command	Op Code	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	Nth Byte
Write Disable	04H	-	-	-	-	-	-
Write Enable	06H	-	-	-	-	-	-
Block Erase (Block size)	D8H	A23-A16	A15-A8	A7-A0	-	-	-
Program Load	02H	A15-A8	A7-A0	D7-D0	Next data	Next data	-
Program Load x4 IO	32H(2)	A15-A8	A7-A0	(D7-D0)x4	Next data	Next data	-
Program Execute	10H	A23-A16	A15-A8	A7-A0	-	-	-
Program Load Random Data	84H(1)	A15-A8	A7-A0	D7-D0	Next data	Next data	-
Program Load Random Data x4 IO	C4H/34H(1)(2)	A15-A8	A7-A0	(D7-D0)x4	Next data	Next data	-
Program Load Random Data Quad IO	72H(1)(2)	A15-A0	(D7-D0)x4	Next data	Next data	Next data	-
Page Read (to Cache)	13H	A23-A16	A15-A8	A7-A0	-	-	-
Read from Cache x1 IO	03H/0BH	A15-A8	A7-A0	Dummy	D7-D0	Next data	Wrap
Read from Cache x2 IO	3BH	A15-A8	A7-A0	Dummy	(D7-D0)x2	Next data	Wrap
Read from Cache x4 IO	6BH(2)	A15-A8	A7-A0	Dummy	(D7-D0)x4	Next data	Wrap
Read from Cache Dual IO	BBH	A15-A0	Dummy	(D7-D0)x2	Next data	Next data	Wrap
Read from Cache Quad IO	EBH(2)	A15-A0	(D7-D0)x4	Next data	Next data	Next data	Wrap
Read ID	9FH	A7-A0	MID	DID	Wrap	Wrap	Wrap
Reset	FFH	-	-	-	-	-	-
Get Feature	0FH	A7-A0	D7-D0	-	-	-	-
Set Feature	1FH	A7-A0	D7-D0	-	-	-	-

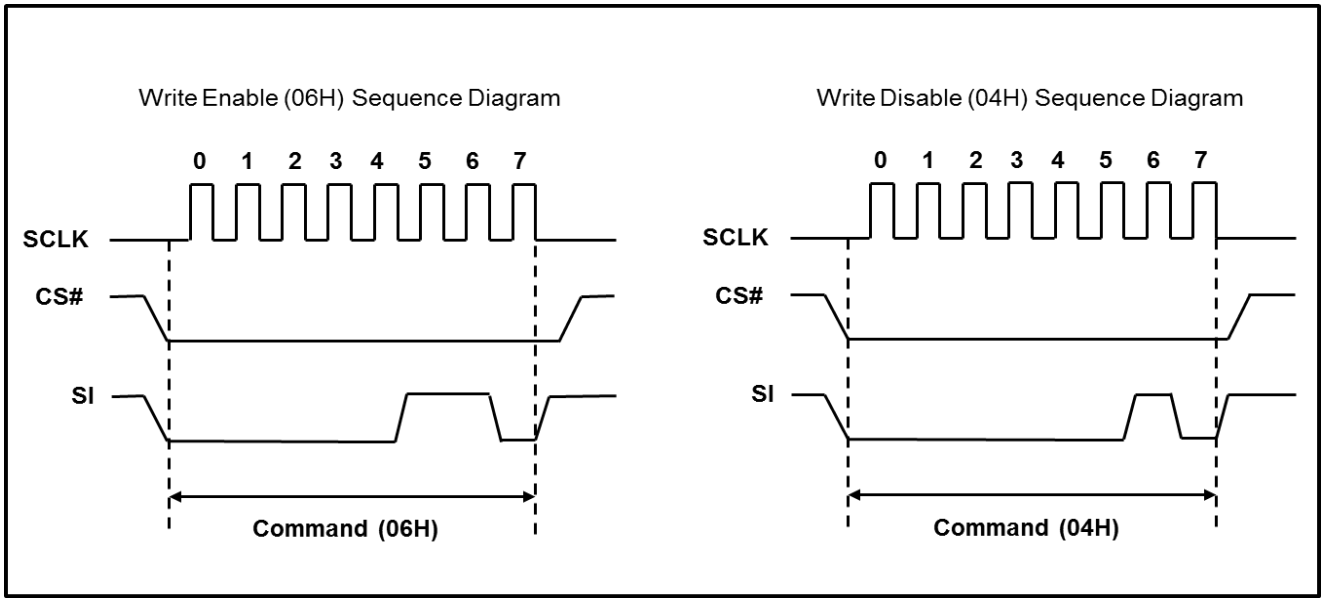
Notes:

1. These commands are only available in Internal Data Move operation.
2. Quad Enable (QE) bit needs to be set to 1 when these commands are issued.

Write Enable Operations

The WRITE ENABLE (WREN, 06H) command is for setting the Write Enable Latch (WEL) bit. The WRITE DISABLE (WRDI, 04H) command is for clearing the WEL bit.

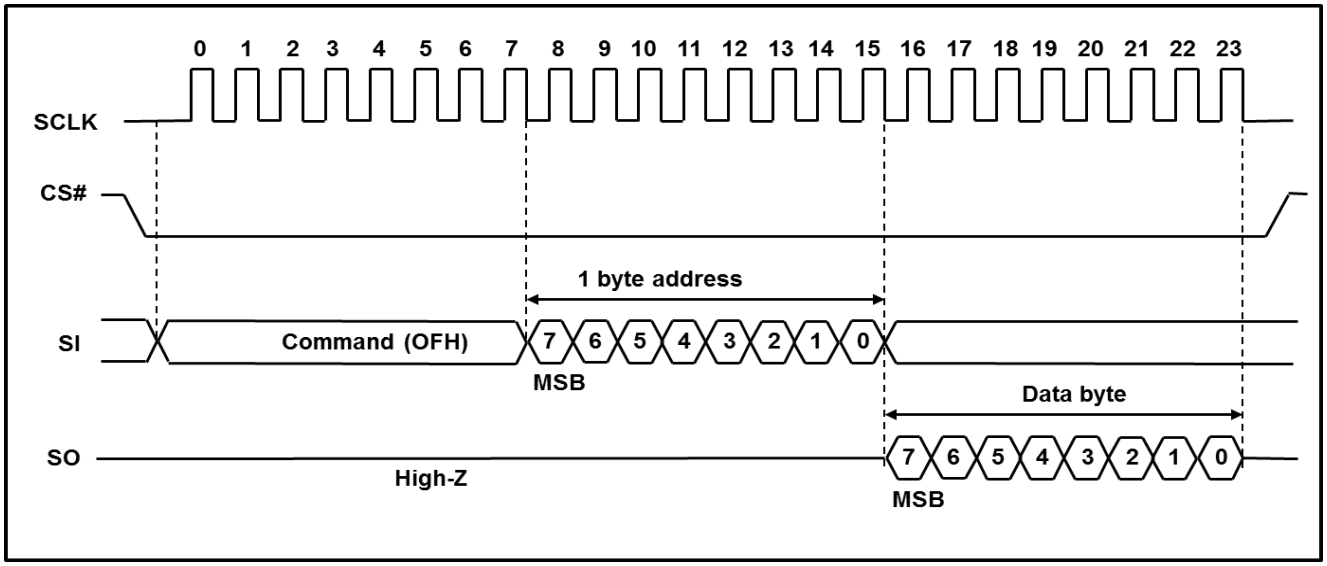
As with any command that changes the memory contents, the WRITE ENABLE command must be executed at first in order to set the WEL bit to 1. Refer to the PAGE READ operation sequence, PAGE PROGRAM operation sequence, Internal Data Move operation sequence, BLOCK ERASE operation sequence and OTP operation sequence.



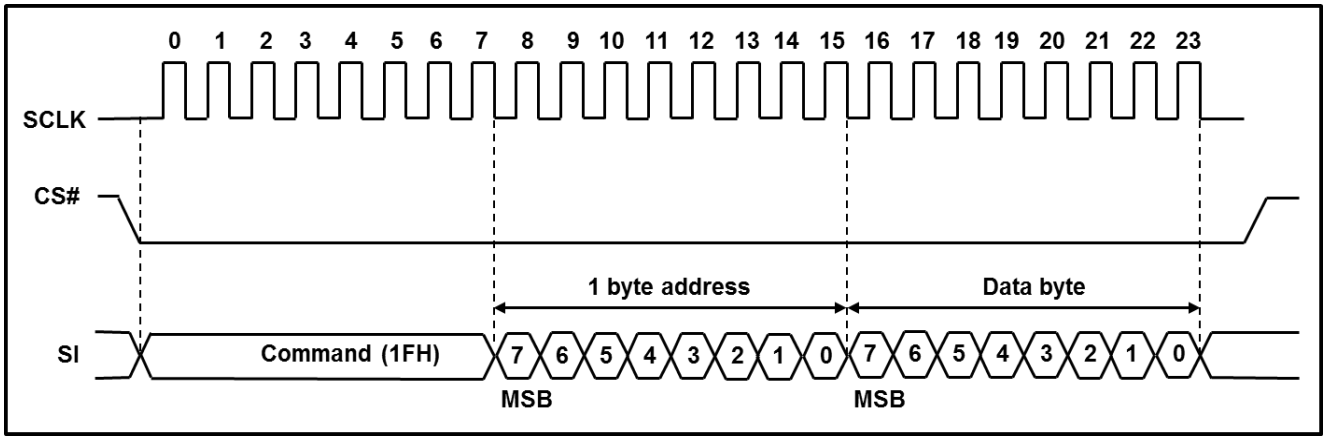
Feature Operation

The GET FEATURE (0FH) and SET FEATURE (1FH) commands are used to monitor the devices status and alter the device behavior.

Get Feature (0FH) Sequence Diagram



Set Feature (1FH) Sequence Diagram



Feature Register Table

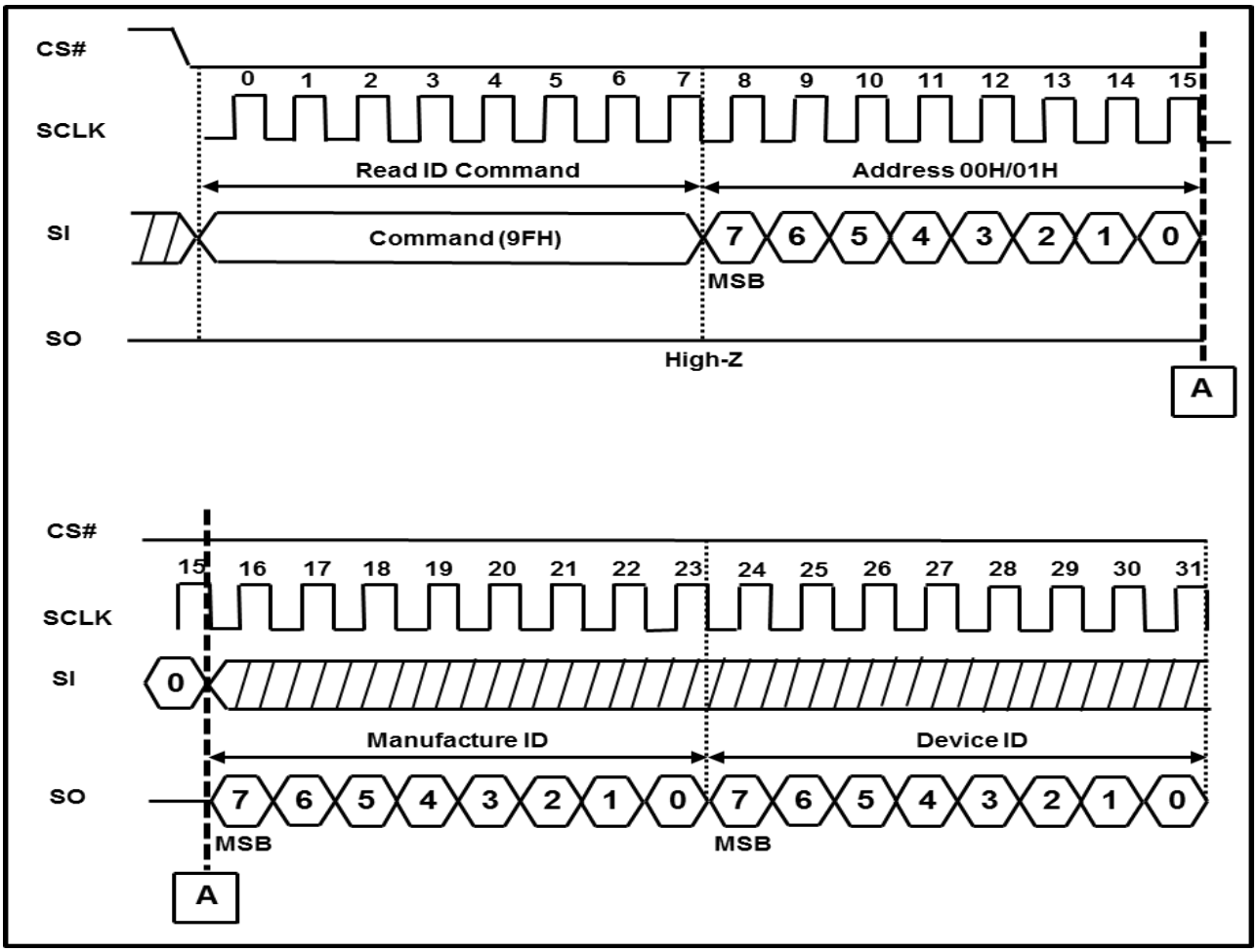
Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block Lock	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
OTP	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	Reserved	Reserved	Reserved	QE
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP

Read ID Operations

Read ID (9FH)

The READ ID command is used to identify the SPI NAND Flash memory device. The Read ID command outputs the manufacture ID with address byte 00H and outputs the device ID when address byte is 01H.

Read ID (9FH) Sequence Diagram



ID Definition Table

Address	Value	R/W	Description
00H	C9h	R	Manufacture ID
01H	22h	R	Device ID

Read Operations

The PAGE READ (13H) command transfers the data from the NAND Flash array to the cache memory. The command sequence is follows:

I. 13H (PAGE READ to Cache)

II. 0FH (GET FEATURE command to read the status)

III. Read from Cache memory

- 03H or 0BH (Read from Cache x1 IO)/3BH (Read from Cache x2 IO)/6BH (Read from Cache x4 IO)
- BBH (Read from Cache Dual IO)/EBH (Read from Cache Quad IO)

The PAGE READ command requires a 24-bit address consisting of dummy bits and block/page address bits. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tRD time. During the busy time, the GET FEATURE command needs to be issued to monitor the status of PAGE READ. After finishing the PAGE READ successfully, the Read from Cache command can be issued in order to read the data out of the cache. The Read from Cache command requires 16 bits of column address which is consisting of wrap bits and column address bits. The number of bits of column address is depends on the page size in different flash. Refer to figures below to view the entire READ operation.

Value of wrap bit is defined as the table bellows,

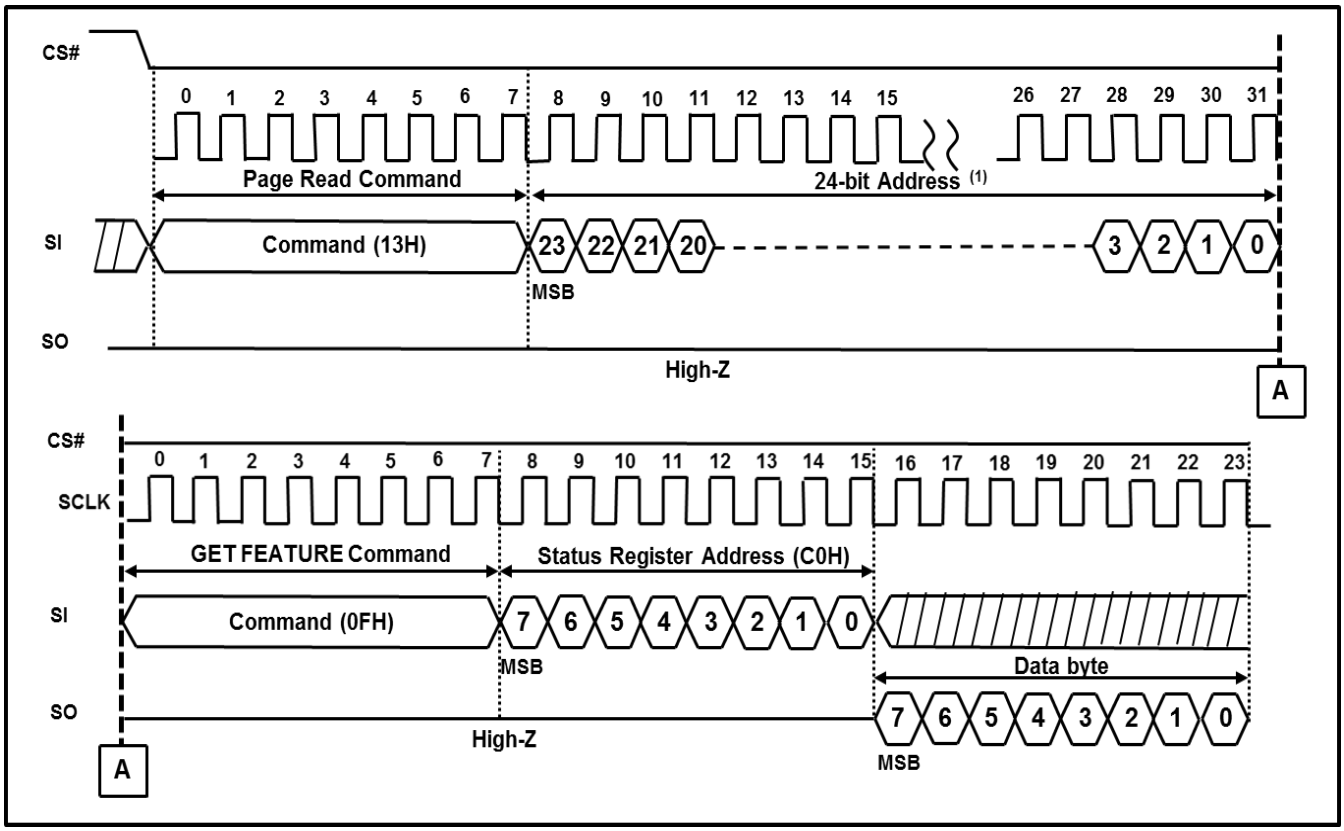
Wrap Bit Table (2K/page)

Wrap <3>	Wrap <2>	Wrap <1>	Wrap <0>	Wrap Length (Byte)
0	0	X	X	2112
0	1	X	X	2048
1	0	X	X	64
1	1	X	X	16

PAGE READ to Cache (13H)

The waveform of PAGE READ to Cache (13H) is as follows,

PAGE READ to Cache (13H) Sequence Diagram

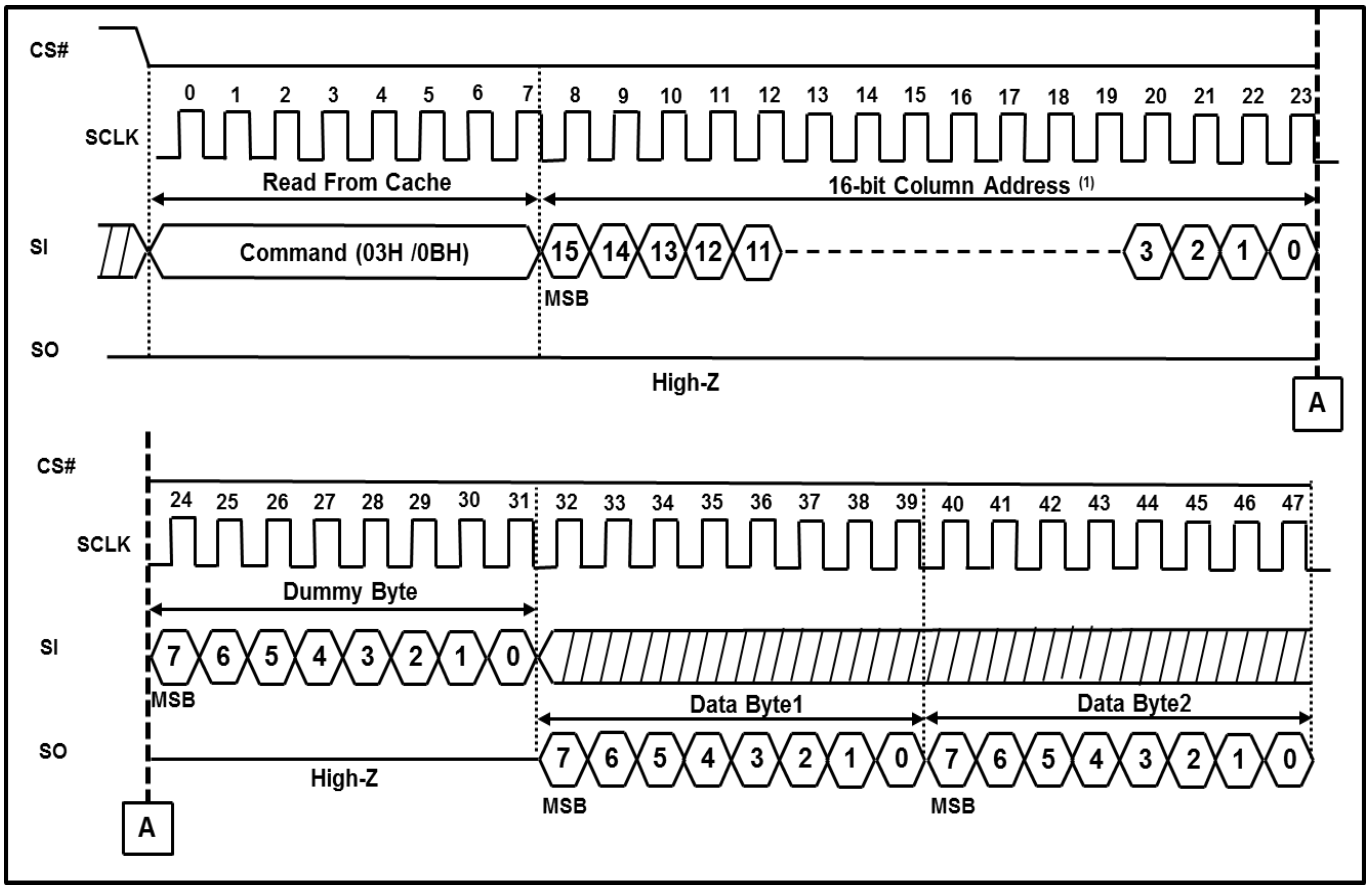


Note : If # of Block = 2048, 24-bit address consists of 7 dummy bits and 17 page/block address bits.

Read from Cache x1 IO (03H/0BH)

The Read from Cache x1 IO (03H/0BH) consists of an OP code followed by 16-bit column address. The column address is composed of wrap bits and column address bits. Refer the Read from Cache x1 IO sequence diagram as follows,

Read from Cache x1 IO (03H/0BH) Sequence Diagram

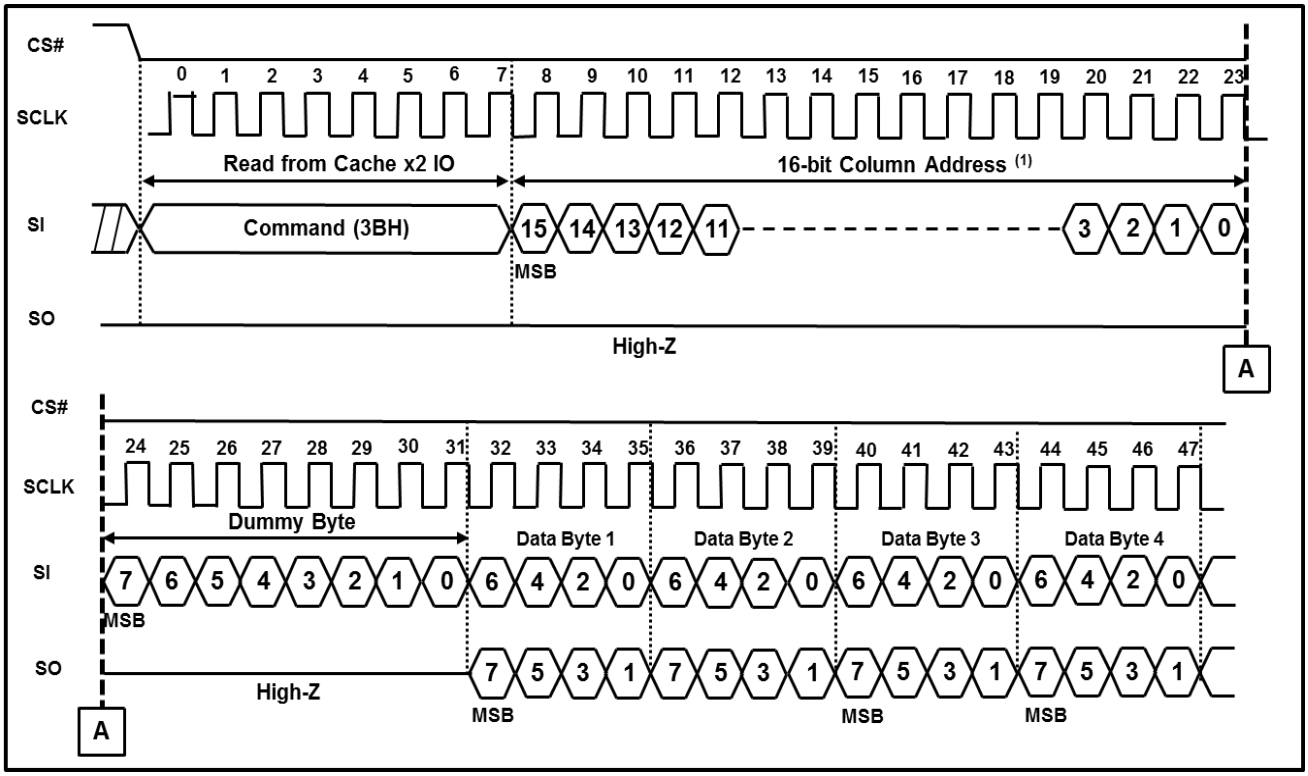


Note : 1 Page = 2K+64B, 16-bit column address consists of 4 wrap bits and 12 column address bits.

Read from Cache x2 IO (3BH)

The Read from Cache x2 IO (3BH) command is similar to the Read from Cache x1 IO (03H/0BH) but the command uses two pins to output data. The data output pins include the SI (SIO0) and SO (SIO1). Refer the Read from Cache x2 IO (3BH) sequence diagram bellowed.

Read from Cache x2 IO (3BH) Sequence Diagram

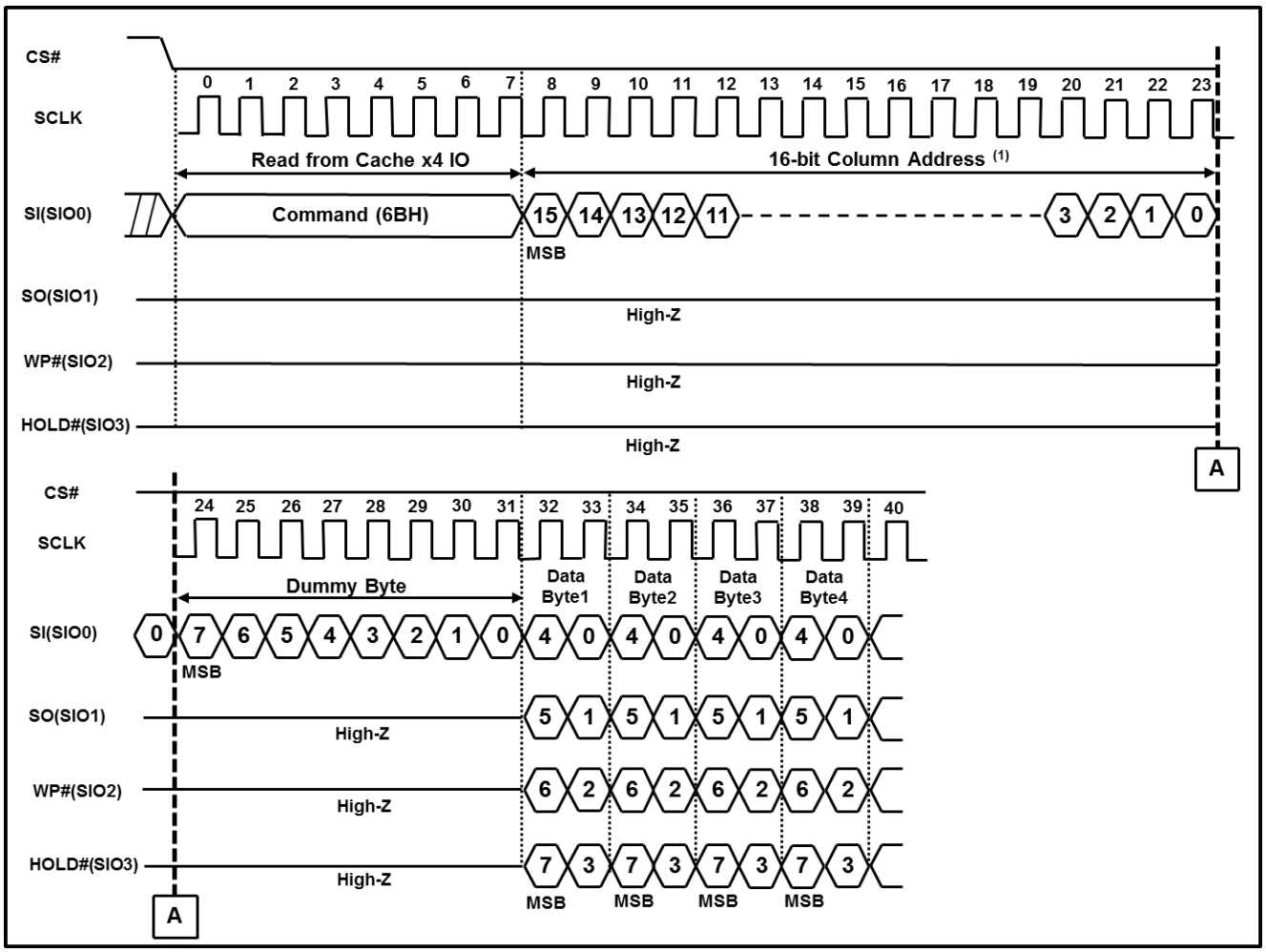


Note : 1 Page = 2K+64B, 16-bit column address consists of 4 wrap bits and 12 column address bits.

Read from Cache x4 IO (6BH)

The Read from Cache x4 IO (6BH) command is similar to the Read from Cache x1 IO (03H/0BH) and the Read from Cache x2 IO (3BH) but the command uses four pins to output data. The four pins include the SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3).The Quad Enable bit (QE) of OTP register (B0[0]) must be set to enable the Read from Cache Quad IO (EBH) command . Refer the Read from Cache x4 IO (6BH) sequence diagram bellowed.

Read from Cache x4 IO (6BH) Sequence Diagram

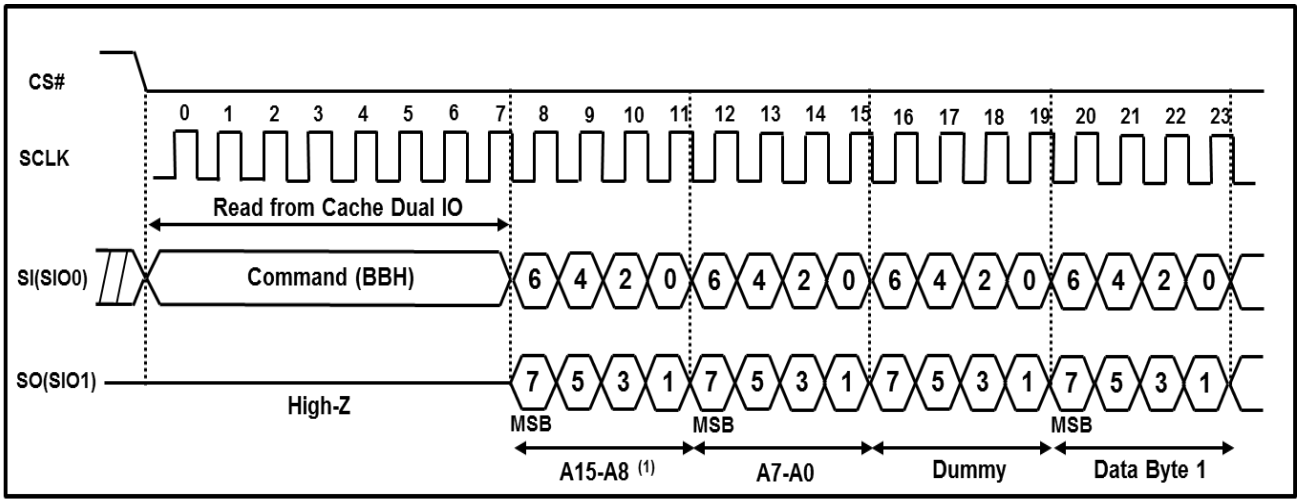


Note : 1 Page = 2K+64B, 16-bit column address consists of 4 wrap bits and 12 column address bits.

Read from Cache Dual IO (BBH)

The Read from Cache Dual IO command (BBH) is similar to the Read from Cache x2 IO command (3BH) but using both of SI (SIO0) and SO (SIO1) as input bin. Each bit in 16-bit column address and the followed dummy byte will be latched in during the falling edge of SCLK, then the cache contents will be shifted out 2-bit in a clock cycle through the SI (SIO0) and SO (SIO1).

Read from Cache Dual IO (BBH) Sequence Diagram

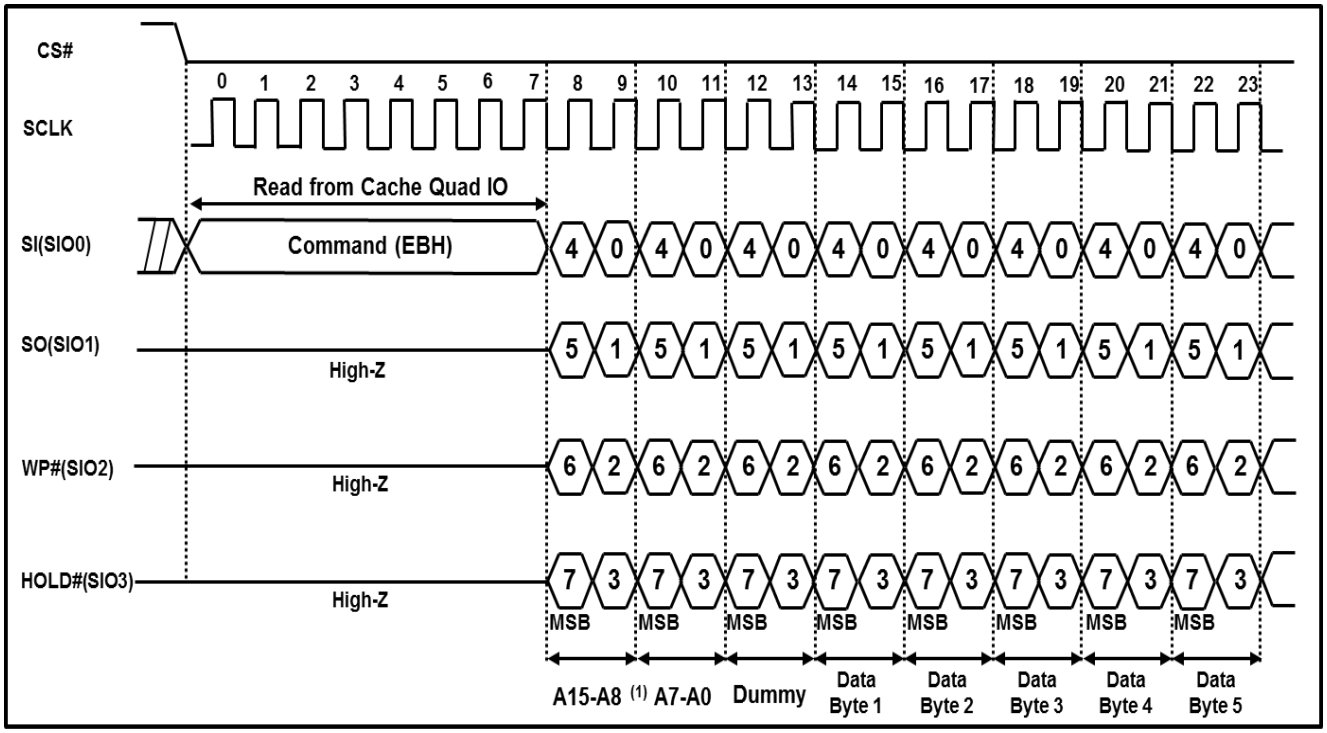


Note : 1 Page = 2K+64B, 16-bit column address consists of 4 wrap bits and 12 column address bits.

Read from Cache Quad IO (EBH)

The Read from Cache Quad IO (EBH) command is similar to the Read from Cache x4 IO (6BH) command but with 4 input pins which include SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3). Each bit in 16-bit column address and the followed dummy byte will be latched in during the raising edge of SCLK through these four input pins, and then the cache contents will be shifted out 4-bit in a clock cycle through the SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3). The Quad Enable bit (QE) of OTP register (B0[0]) must be set to enable the Read from Cache Quad IO (EBH) command .

Read from Cache Quad (EBH) Sequence Diagram



Note : 1 Page = 2K+64B, 16-bit column address consists of 4 wrap bits and 12 column address bits.

Program Operations

The PAGE PROGRAM sequence is transfer the data from the host to NAND Flash array through cache memory. The operation sequence programs the first byte to last byte of data within a page. If more than page size, then those additional bytes are ignored by the cache memory. The PAGE PROGRAM sequence is as follows:

I. 06H (WRITE ENABLE when WEL bit is 0)

II. PROGRAM LOAD

- 02H(PROGRAM LOAD) / 32H(PROGRAM LOAD x4)

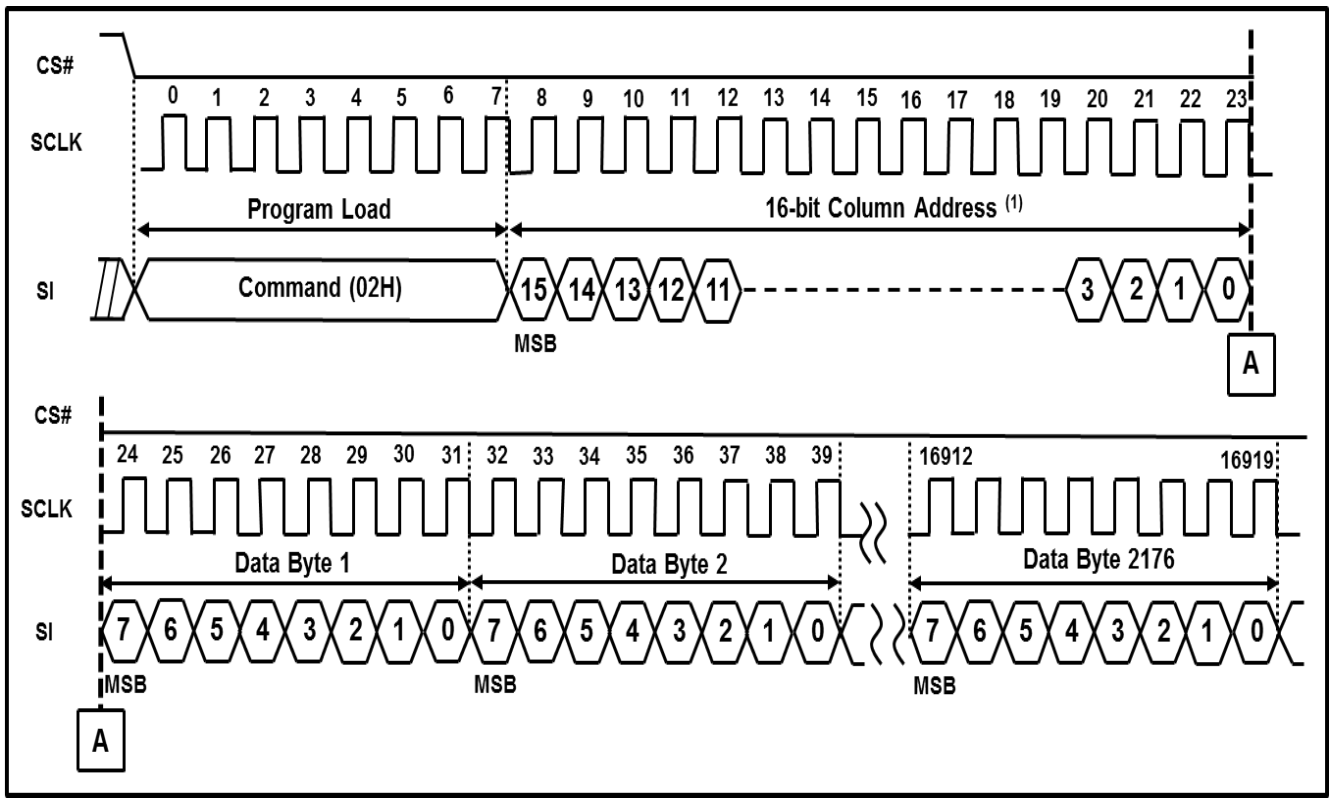
III. 10H (PROGRAM EXECUTE)

IV. 0FH (GET FEATURE command to read the status)

At first, the WRITE ENABLE (06H) command is used to set the Write Enable Latch (WEL) bit The Write Enable Latch (WEL) bit must be set prior to program execute (10h). The PROGRAM LOAD (02H/32H) command is issued then and the PROGRAM LOAD command can only be issued one time in a PAGE PROGRAM sequence. Secondly, the PROGRAM EXECUTE (10H) command is issued to program the data into the page. During the busy time, the GET FEATURE command needs to be issued to monitor the status of PAGE PROGRAM. After finishing the PAGE PROGRAM successfully, the OIP and WEL bit in status register (C0H) will be set to 0.

Program Load (PL) (02H)

Program Load (02H) Sequence Diagram

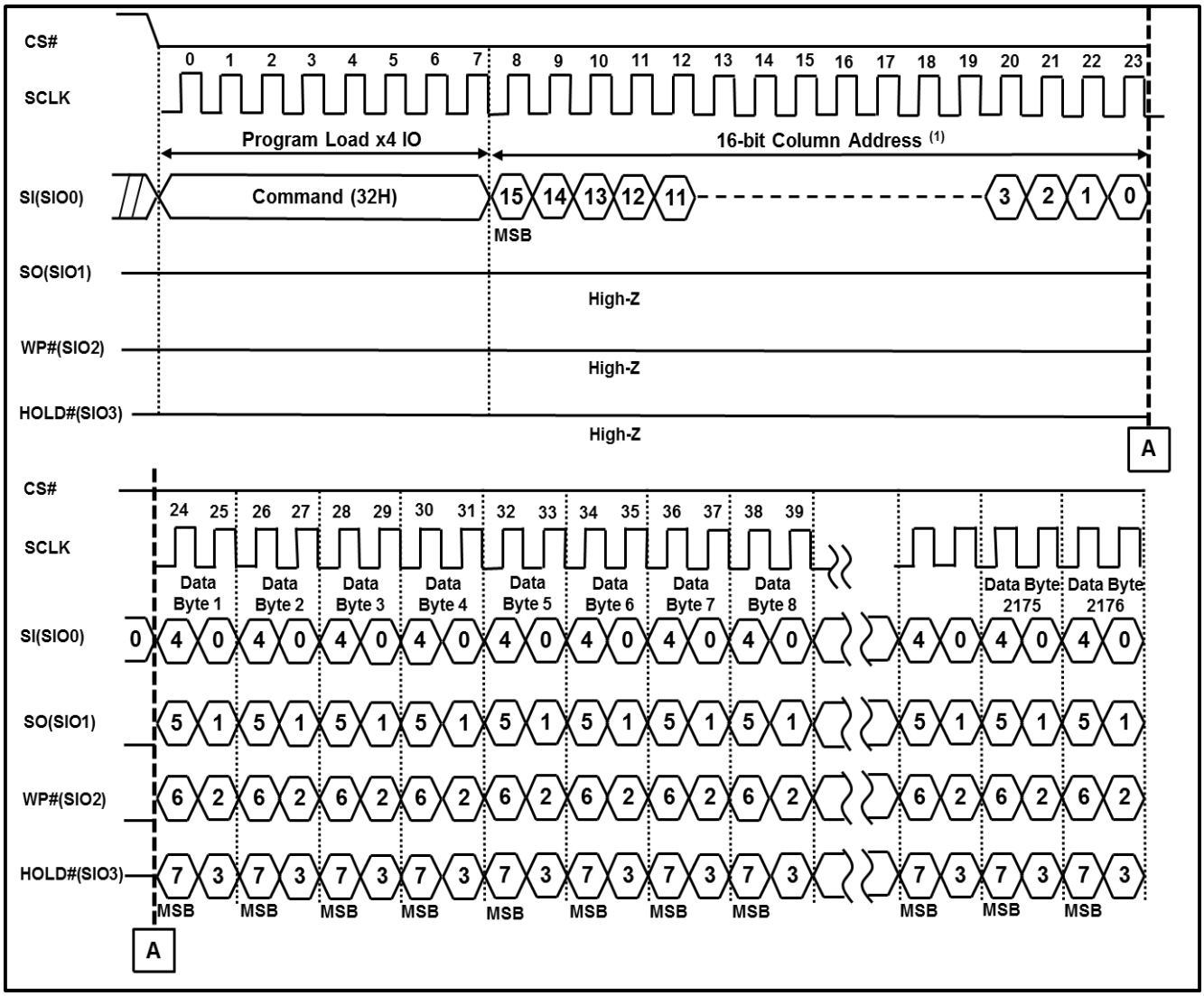


Note : 1 Page = 2K+64B, 16-bit column address consists of 4 wrap bits and 12 column address bits.

Program Load x4 IO (PL x4) (32H)

The PROGRAM LOAD x4 IO (32H) command is similar to the PROGRAM LOAD (02H) command but with four input pins to transfer data in. The four input pins are SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3). The Quad Enable bit (QE) of OTP register (B0[0]) must be set to enable the PROGRAM LOAD x4 IO (32H) command. The command sequence is shown below,

Program Load x4 IO (32H) Sequence Diagram

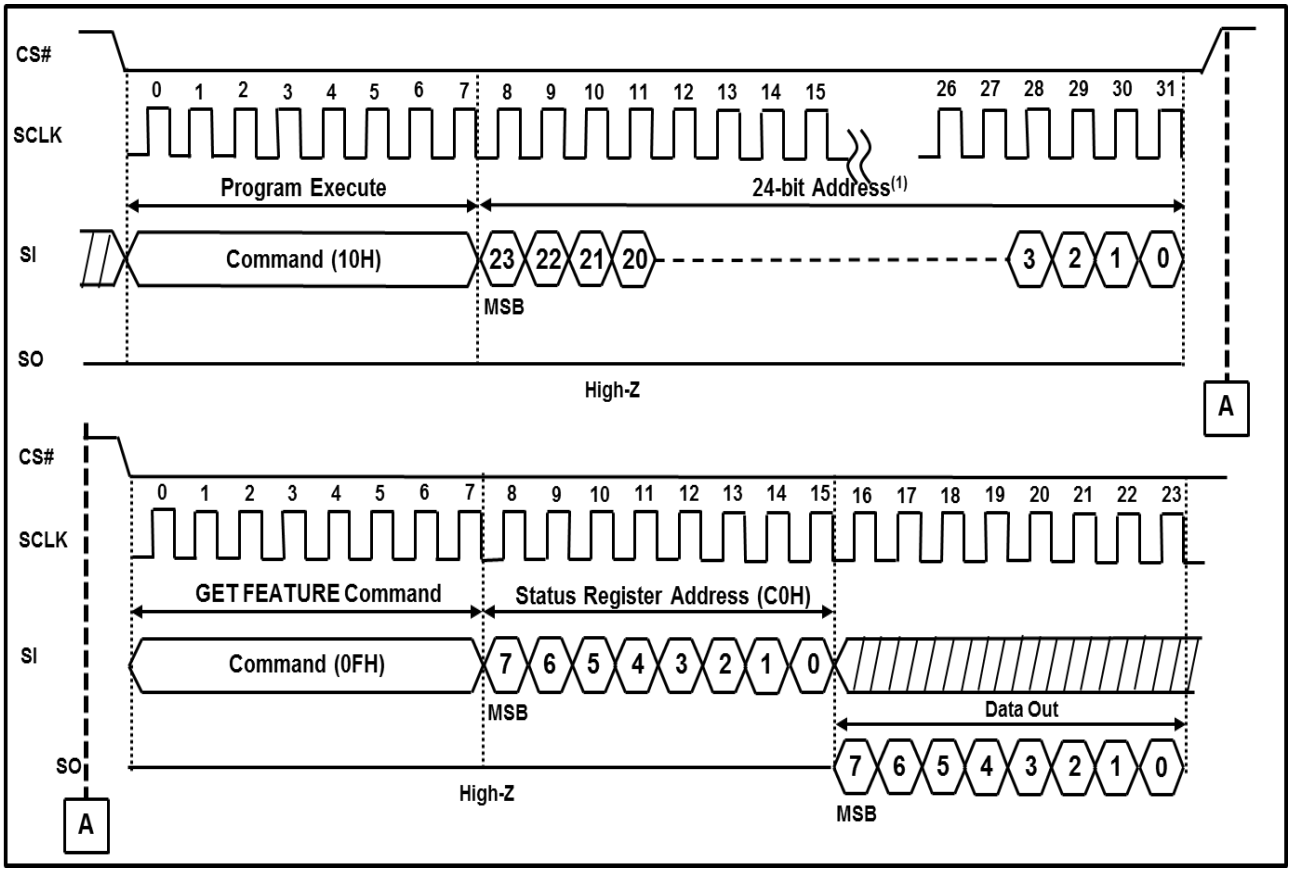


Note : 1 Page = 2K+64B, 16-bit column address consists of 4 wrap bits and 12 column address bits.

Program Execute (PE) (10H)

PROGRAM EXECUTE (10H) command must be issued after the data is loaded and the WEL bit be set to HIGH. The PROGRAM EXECUTE (10H) command will transfer data from the cache to the main array. The PROGRAM EXECUTE (10H) consists of an 8-bit Op code, followed by a 24-bit address which including dummy bits and page/block address. This operation needs to wait the busy time. The OIP bit in status register (C0H) will be HIGH until controller finishes the program. The P_FAIL bit in status register (C0H) will be set HIGH if program fail.

Program Execute (10H) Sequence Diagram



Note : If # of Block = 2048, 24-bit address consists of 7 dummy bits and 17 page/block address bits.

Internal Data Move Operation

The Internal Data Move operation sequence programs or replaces data in a page with existing data.

The Internal Data Move operation sequence is as follows:

I. 13H (PAGE READ to cache)

II. 0FH (GET FEATURE command to read the status).

III. Optional 84H/C4H/34H/72H **(PROGRAM LOAD RANDOM DATA. The command of Program load random data can be operated several times in this step.)

IV. 06H (WRITE ENABLE)

V. 10H (PROGRAM EXECUTE)

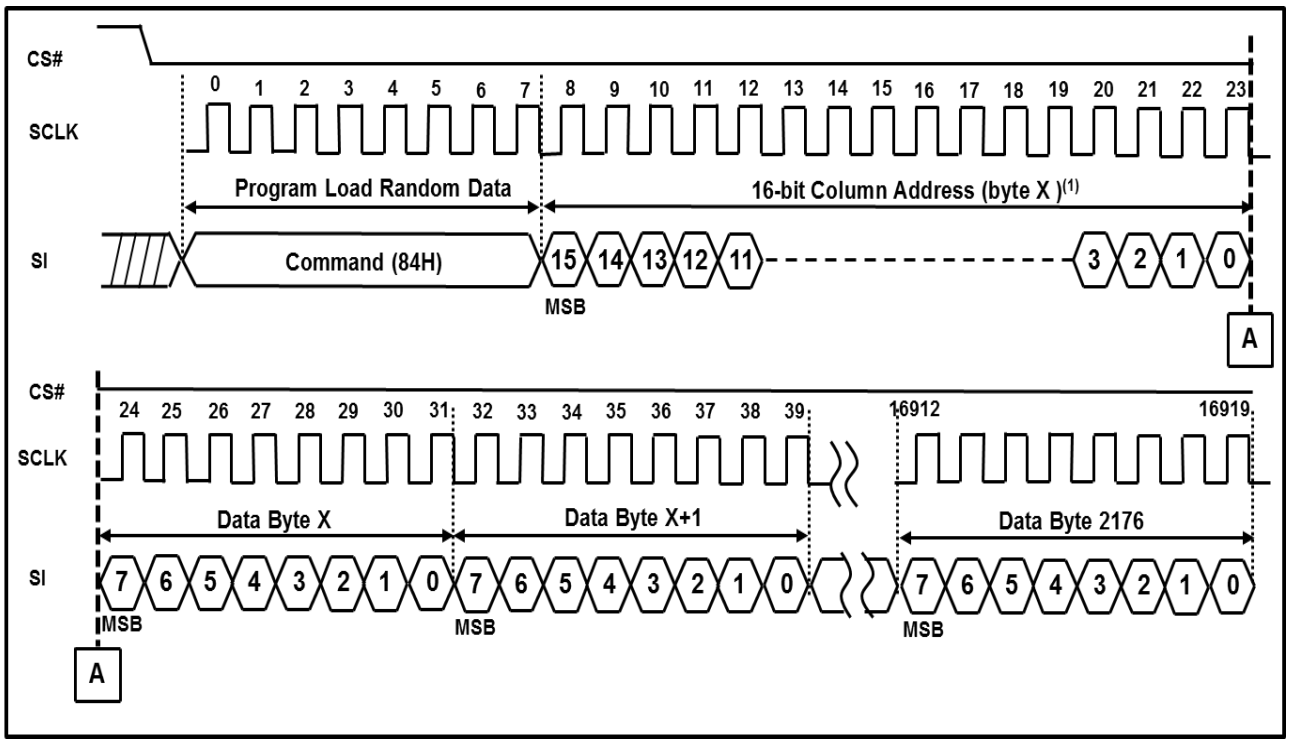
VI. 0FH (GET FEATURE command to read the status)

** 84H/C4H/34H/72H commands are only available in Internal Data Move operation.

Program Load Random Data (84H)

Program Load Random Data (84H) command consists of an OP code, followed by 16 bit column address which composed of dummy bits and column address bits. This command can only be used in Internal Data Move operation sequence.

Program Load Random Data (84H) Sequence Diagram

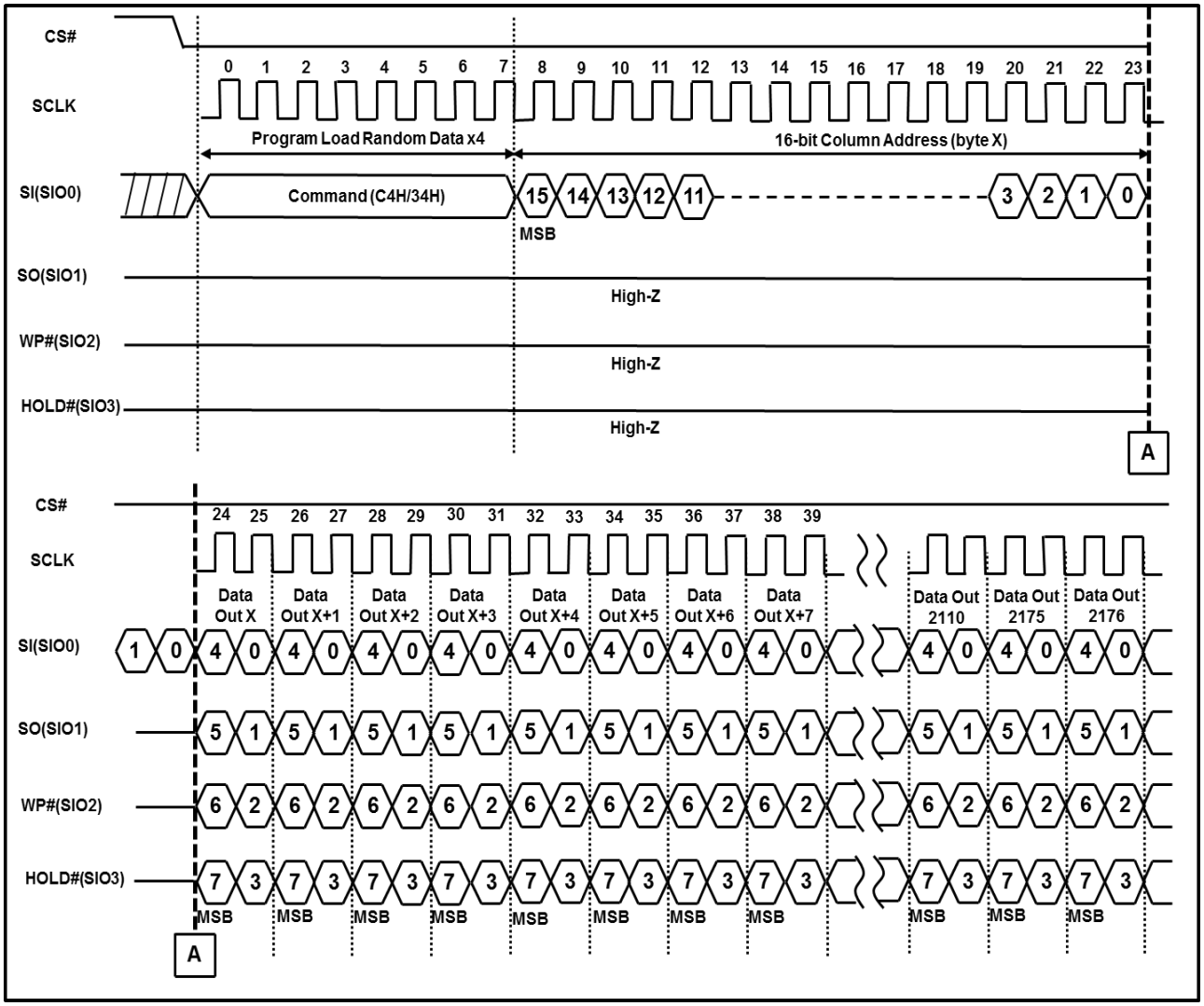


Note : 1 Page = 2K+64B, 16-bit column address consists of 4 wrap bits and 12 column address bits.

Program Load Random Data x4 (C4H/34H)

The Program Load Random Data x4 (C4H/34H) command is similar to the Program Load Random Data Command (84H) but with four input pins. The four input pins are SI(SIO0), SO(SIO1), WP#(SIO2) and HOLD#(SIO3). The Quad Enable bit needs to be set before the Program Load Random Data x4 command be used. The command is only available during the Internal Data Move sequence operation sequence.

Program Load Random Data x4 (C4H/34H) Sequence Diagram

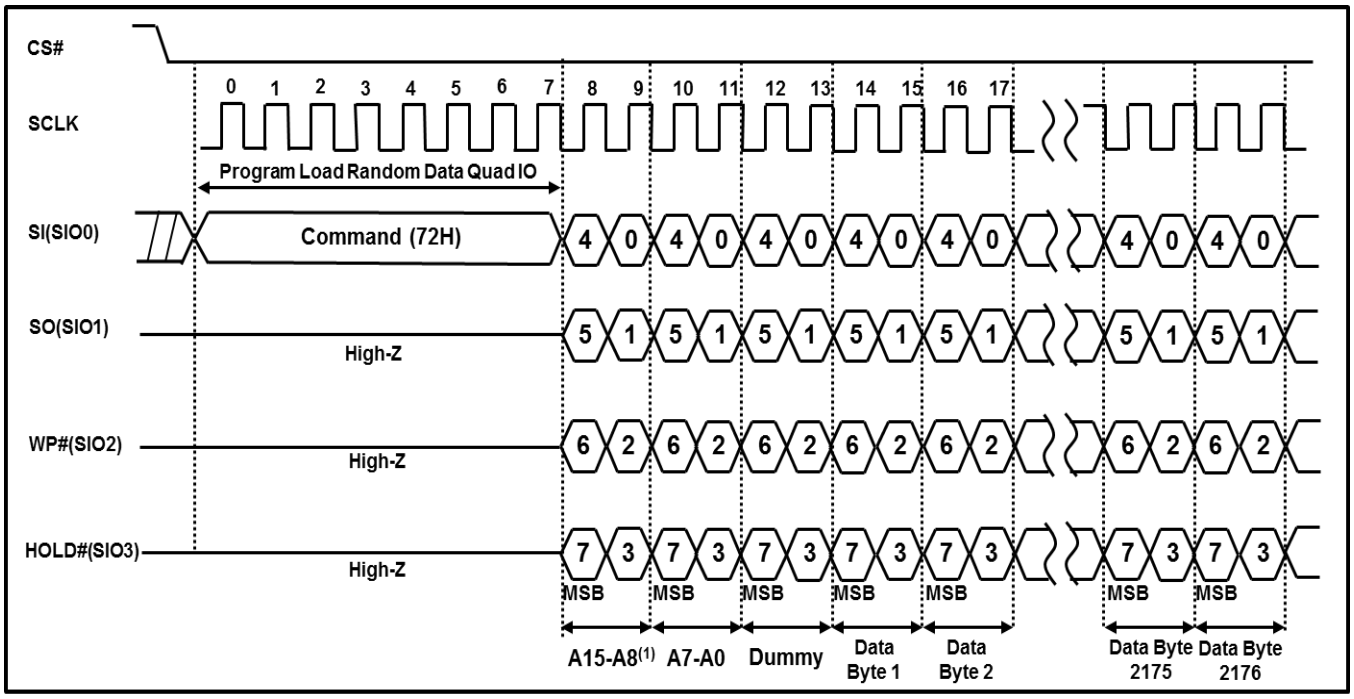


Note : 1 Page = 2K+64B, 16-bit column address consists of 4 wrap bits and 12 column address bits.

Program Load Random Data Quad IO (72H)

The Program Load Random Data Quad IO (72H) is similar to the Program Load Random Data x4 (C4H/34H) command but with 4 input pins: SI(SIO0), SO(SIO1), WP#(SIO2) and HOLD#(SIO3). The Quad Enable (QE) bit in feature register (B0[0]) needs to be set to 1 for the Program Load Random Data Quad IO command. This command is only available during Internal Data Move operation sequence.

Program Load Random Data Quad IO (72H) Sequence Diagram



Note : 1 Page = 2K+64B, 16-bit column address consists of 4 wrap bits and 12 column address bits.

Erase Operation

Block Erase (D8H)

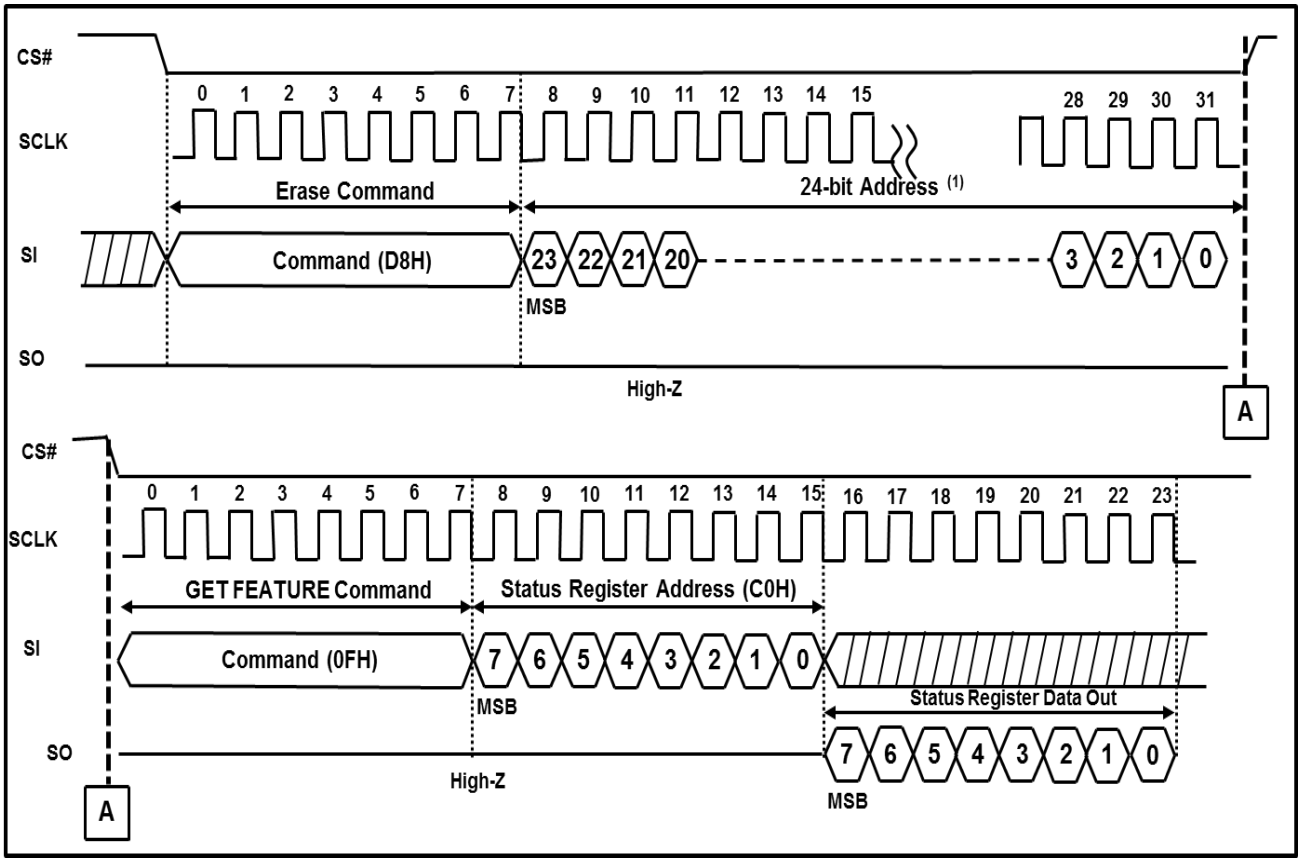
The BLOCK ERASE (D8H) command is used to erase at block level. The command sequence for BLOCK ERASE operation is as follows,

- 06H (WRITE ENABLE command)
- D8H (BLOCK ERASE command)
- 0FH (GET FEATURE command to read the status register)

Erase Operation sequence starts from a WRITE ENABLE (06H) command to set WEL bit to 1. After executing the WRITE ENABLE command, BLOCK ERASE (D8H) command can be issued. BLOCK ERASE (D8H) requires a 24-bit address which consists of dummy bits and row address (page address in row address will be ignored automatically).

Issue the GET FEATURE (0FH) command to monitor the erase operation after issuing the BLOCK ERASE. The E_FAIL bit in status register can reflect whether the block be erased successfully or not.

Block Erase (D8H) Sequence Diagram



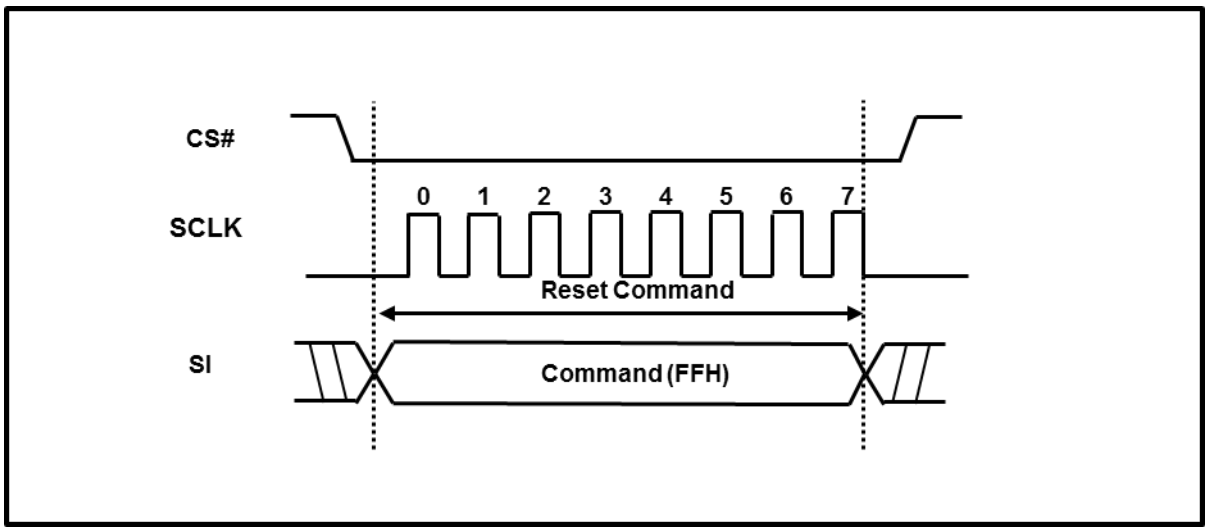
Note : If # of Block = 2048, 24-bit address consists of 7 dummy bits and 17 page/block address bits.

Reset Operation

Reset (FFH)

The RESET (FFH) command stops all operations. For example, the RESET command can stop the previous operation and the pending operations during a cache program or a cache read command.

Reset (FFH) Sequence Diagram



One-Time Programmable (OTP) function

The serial device offers a protected, OTP NAND flash memory area. 4 full pages are available on the device and OTP address is 00H~03H. Users can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0.

OTP States

OTP_PRT	OTP_EN	State
X	0	Normal operation. Cannot access the OTP region.
0	1	Access OTP region. PAGE READ and PAGE PROGRAM are allowed.
1	1	The OTP_PRT has two situations when the device power on, 1. OTP_PRT is 0 when the device power on: User can use SET FEATURE command to set the OTP_PRT and OTP_EN bit to 1, and then issue PROGRAM EXECUTE (10H) to lock OTP region. Once we lock the OTP region, the OTP_PRT will permanently be 1. 2. OTP_PRT is 1 when the device power on: user can only read the OTP region data.

How to access to OTP region

- Issue the SET FEATUTE command (1FH)
- Set Feature bit OTP_EN
- Issue the PAGE READ command or PAGE PROGRAM command The PAGE PROGRAM command only be allowed when OTP_PRT is 0. The PAGE PROGRAM command will automatically be ignored if OTP_PRT is 1.

How to protect OTP region

Only when the following steps are completed, the OTP_PRT will be set to 1

- Issue the SET FEATURE (1FH) command
- Set feature bit OTP_EN and OTP_PRT
- 06H (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10H) command.
- Issue the GET FEATURE (0FH) command to wait the device goes to ready state from busy.

Block Protection

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE commands. After power-up, the device is in the “locked” state, i.e., feature bits BP0, BP1 and BP2 are set to 1, INV, CMP and BRWD are set to 0.

Some block operations related to the block protection are listed as below,

- SET FEATURE command must be issued to alter the state of protection feature bit
- When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set.
- When a PROGRAM/ERASE command is issued to a locked block, status bit OIP in status register (C0H) remains 0. The status register (C0H) will return 04H when a PROGRAM command is issued to program a locked block. The status register (C0H) will return 08H when an ERASE command is issued to erase a locked block.
- When WP# is not LOW, user can issue SET FEATURE command and use the protection register (A0H) and the block protect bits table below to alter the protection rows.

Block Protect Bits Table

CMP	INV	BP2	BP1	BP0	Protect Rows
X	X	0	0	0	All unlocked
0	0	0	0	1	Upper 1/64 locked
0	0	0	1	0	Upper 1/32 locked
0	0	0	1	1	Upper 1/16 locked
0	0	1	0	0	Upper 1/8 locked
0	0	1	0	1	Upper 1/4 locked
0	0	1	1	0	Upper 1/2 locked
X	X	1	1	1	All locked (Default)
0	1	0	0	1	Lower 1/64 locked
0	1	0	1	0	Lower 1/32 locked
0	1	0	1	1	Lower 1/16 locked
0	1	1	0	0	Lower 1/8 locked
0	1	1	0	1	Lower 1/4 locked
0	1	1	1	0	Lower 1/2 locked
1	0	0	0	1	Lower 63/64 locked
1	0	0	1	0	Lower 31/32 locked
1	0	0	1	1	Lower 15/16 locked
1	0	1	0	0	Lower 7/8 locked
1	0	1	0	1	Lower 3/4 locked
1	0	1	1	0	Block 0
1	1	0	0	1	Upper 63/64 locked
1	1	0	1	0	Upper 31/32 locked
1	1	0	1	1	Upper 15/16 locked
1	1	1	0	0	Upper 7/8 locked
1	1	1	0	1	Upper 3/4 locked
1	1	1	1	0	Block 0

Status Register

The content of status register can be read by issuing the GET FEATURE (0FH) command, followed by the status register address C0H. The meaning of each Bit in status register is as the table below,

Status Register Bit Description

Bit	Name	Description
P_FAIL	Program Fail	This bit indicates that a program failure has occurred. It will also be set if the user attempts to program an invalid address or a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command.
E_FAIL	Erase Fail	This bit indicates that an erase failure has occurred. It will also be set if the user attempts to erase a locked region. This bit is cleared at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	Write Enable Latch	This bit indicates that the current status of the write enable latch(WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	This bit is set when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.
ECCS1, ECCS0	ECC Status	ECC status as follows 00b = No bit errors were detected 01b = bit error was detected and corrected 10b = bit error was detected and not corrected 11b = bit error was detected and corrected, error bit number = ECC max which is according to extended register. ECCS is set to 00b either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid operation. After power-on RESET, ECC status is set to reflect the contents of block 0, page 0.

ECC (Internal)

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

The SPI NAND offers data corruption protection by offering optional internal ECC. READ and PROGRAM with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the “active” state. To enable/disable ECC, perform the following command sequence:

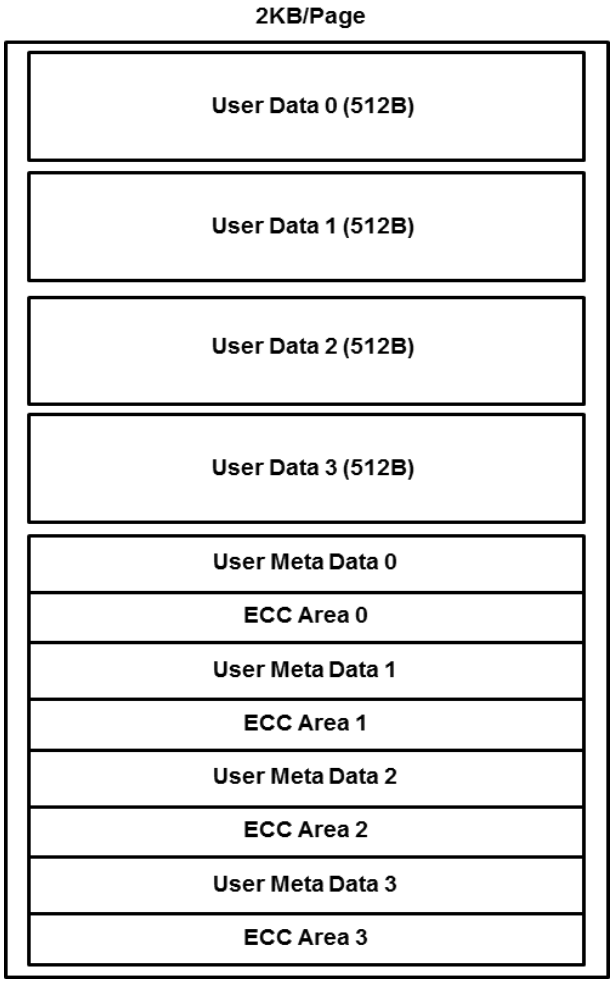
- Issue the SET FEATURES command (1FH) and then set the feature bit ECC_EN likes below,

1. To enable ECC, Set ECC_EN to 1.
2. To disable ECC, Clear ECC_EN to 0.

With internal ECC, the user must accommodate the following

- Spare area definition provided in the ECC Protection table below
- ECC can protect according user and meta data. Writes to the ECC area are ignored.

ECC Protection and Spare Area for 2KB/Page



2KB/Page and ECC

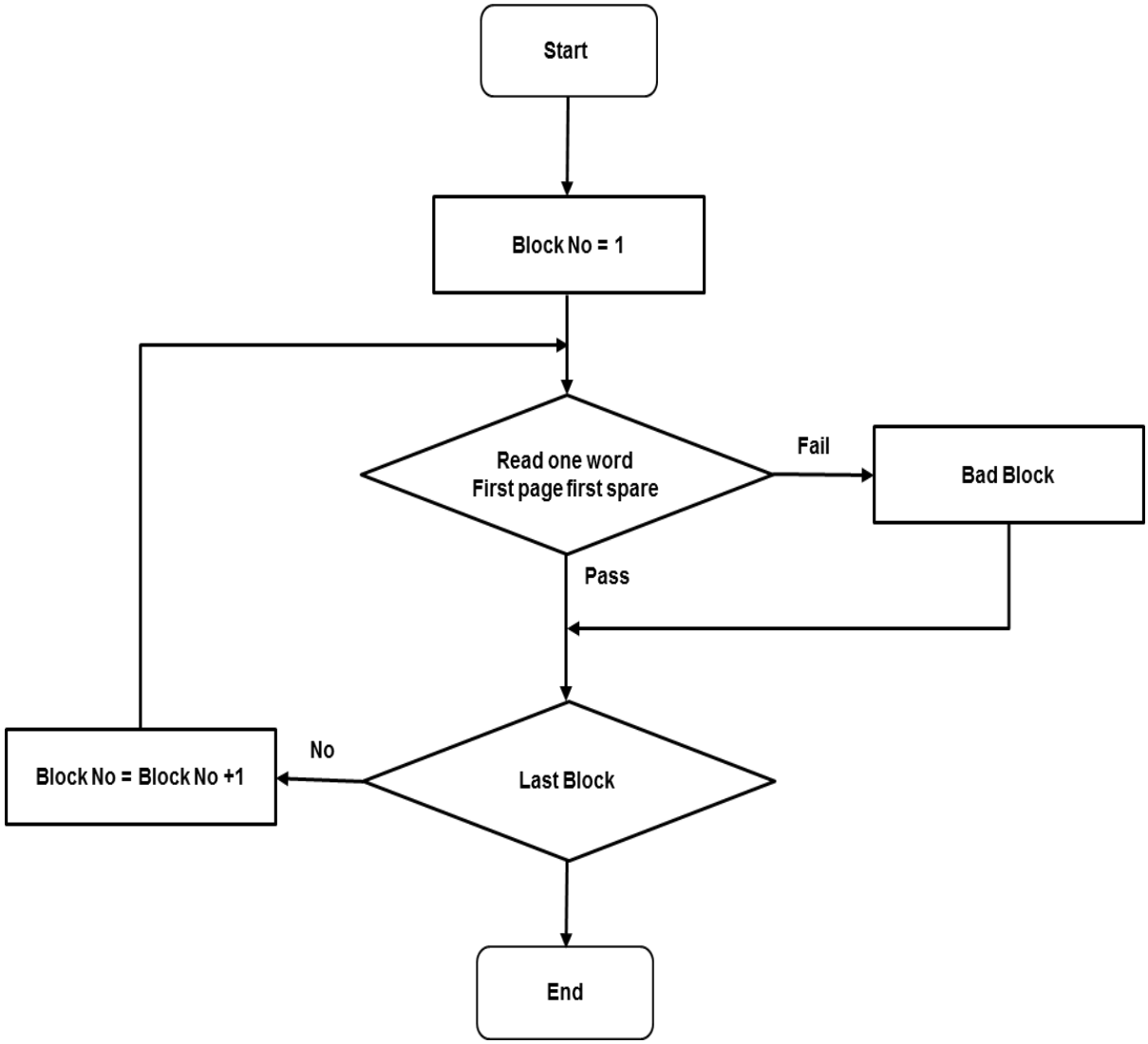
Page Size	Spare Size	ECC Cap	User Data	Meta Data	ECC Data	Unprotected Data
2048 Bytes	64 Bytes	4 Bits	512 Bytes x4	8 Bytes x4	8 Bytes x4	1st to 4th byte in meta data are unprotected by ECC.

Note:

The ECC protection in meta data area can also be set to “All bytes in meta data are protected by ECC” and If user want to other internal ECC mode(2, 4, 6), please contact “HeYangTek” for details.

Invalid block (bad block)

The device occasionally contains unusable blocks. Please read one word of first page of first spare in each block. HY makes sure that every invalid block has data at this word. If the data of the word is “0”, define the block as a bad block. Please don’t perform an program/erase operation to bad blocks. SPI NAND will abort any operation with bad blocks.

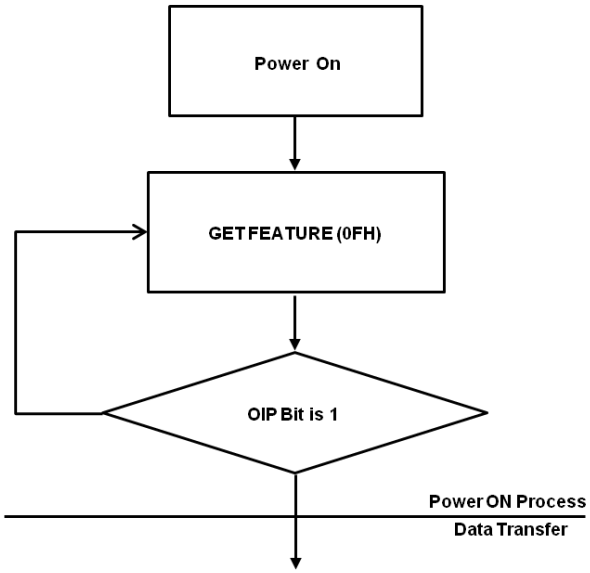


Power-On Process

The power on process starts with GET FEATURE (0Fh). SPI NAND will use the OIP bit in the status register to inform the host that initialization in power-on process is completed. Setting OIP bit to1 indicates that the SPI NAND is still initializing. Setting the OIP bit to 0 indicates that the power on process is finished. If OIP bit is 1, the host will repeatedly issues GET FEATURE (0Fh) command to monitor the power-on process until the OIP bit is set to 0.

When OIP is 0 (after Power-On) , SPI NAND will auto-read 2KB data into “Cache memory” form block0, page0.

Flow Chart of Power-On Process



Programming and Erasing Characteristics

Programming, Erasing & block Characteristics				
Parameters	**Min**	**Typical**	**Max**	**Unit**
Read from flash into cache	120	150		us
One block erase		2.5		ms
Program from cache to flash		600		us

DC Characteristics

3.3V SPI NAND Flash					
Parameters	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
SPI Supply Voltage(VCCAH)	V_IH	2.9	3.3	3.6	V
Input Leakage Current	I_LI			10	uA
Output Leakage Current	I_LO			10	uA
Operation current (read)	I		30	40	mA

AC Time Characteristics (C_{Load} = 30uF)

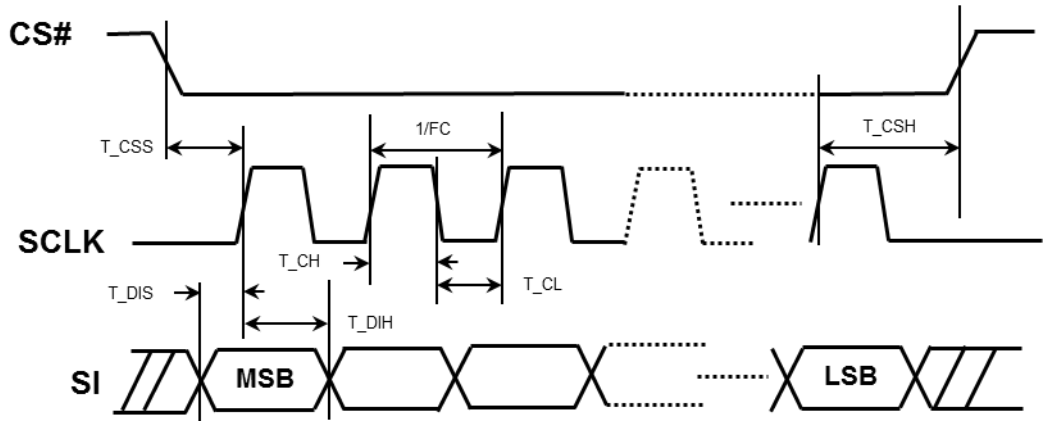
(T = -40 ~ 85°C,V = 2.9 ~ 3.6V, C_L = 30pF)

Parameters	Symbol	Min	Typical	Max	Unit
Clock Frequency for 3.3v	FC		60	80	MHz
Clock High Time	T_CH	4.8			ns
Clock Low Time	T_CL	4.8			ns
CS# Setup Time	T_CSS	2			ns
CS# Hold Time	T_CSH	4			ns
Data In Setup Time	T_DIS	2			ns
Data In Hold Time	T_DIH	2			ns
Clock Low to Output Valid	T_CLO		4		ns
CS# High to Output Invalid	T_CSDI			2	ns

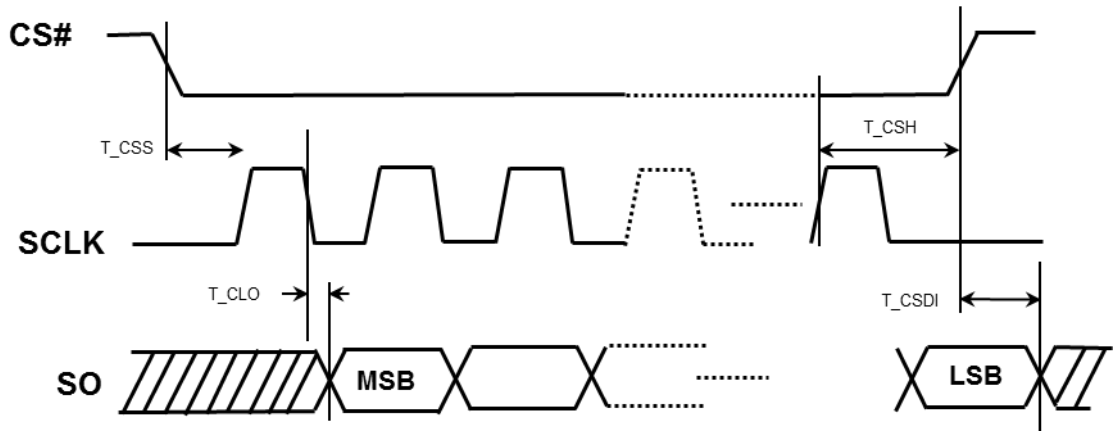
Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature	-40 ~ 85	℃
Stroage Temperature	-55 ~ 125	℃
Applied Input/Output Voltage	VCC + 0.4	V

Serial Input Timing

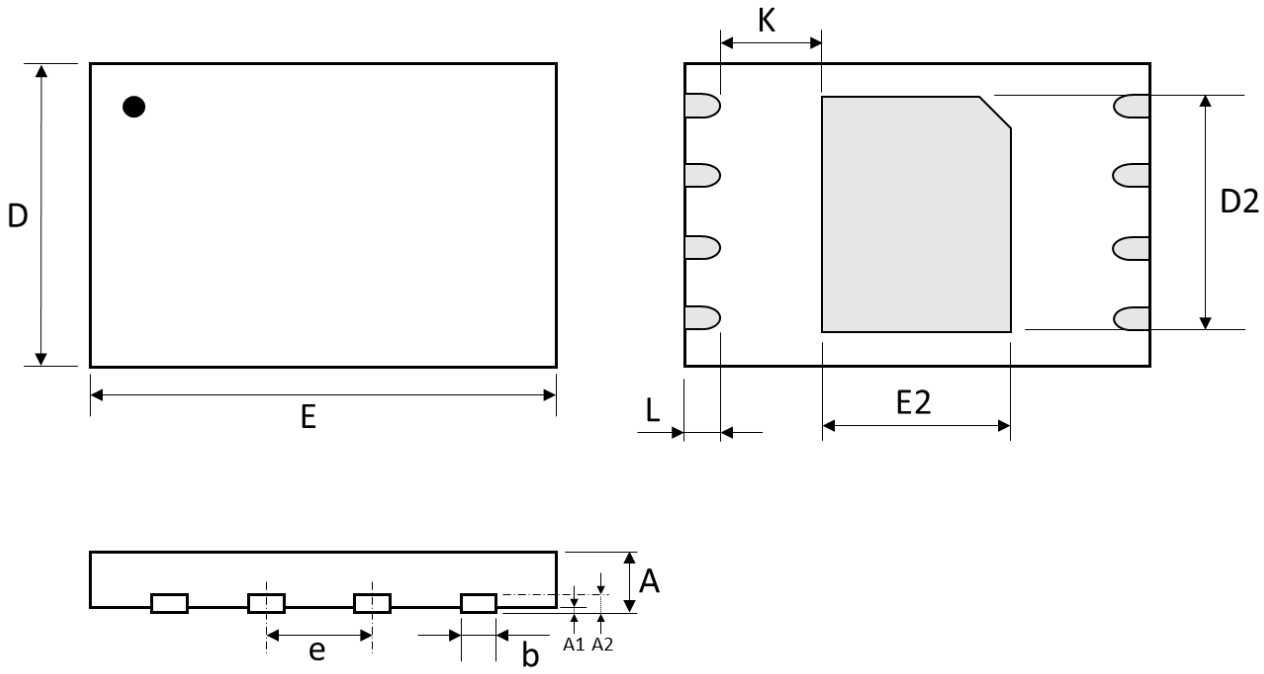


Serial Output Timing



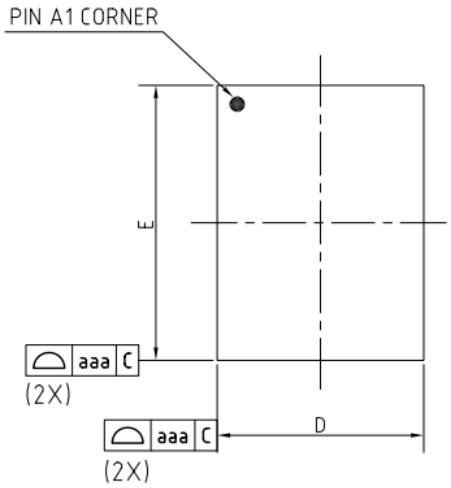
Package Outline

WSON8:

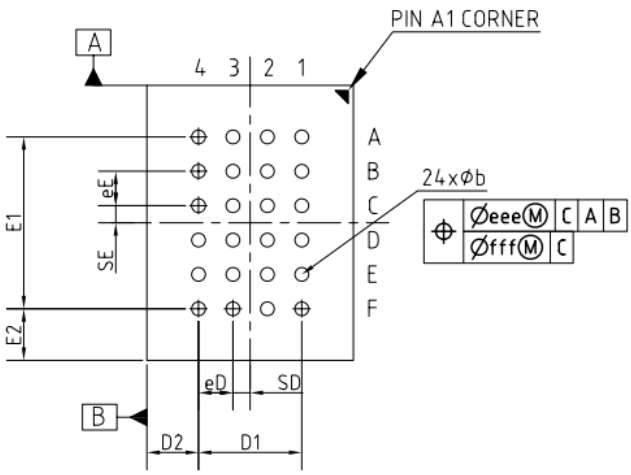


SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203 REF.		
b	0.35	0.40	0.45
D	5.90	6.00	6.10
E	7.90	8.00	8.10
e	1.27 BSC		
L	0.45	0.50	0.55
K	0.20	_	_
D2	4.25	4.30	4.35
E2	3.35	3.40	3.45

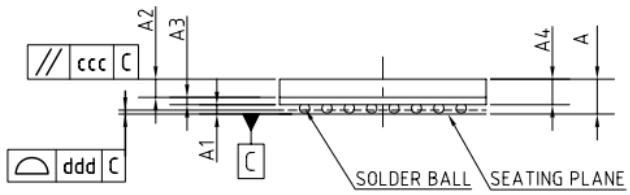
24-Ball TFBGA:



Top View



Bottom View



Side View

ITEM.		SYM.	DIMENSION (mm)			ITEM.		SYM.	DIMENSION (mm)		
			MIN.	NOM.	MAX.				MIN.	NOM.	MAX.
Body Size	X	D	5.90	6.00	6.10	Package Edge Tolerance		aaa	---	0.10	---
	Y	E	7.90	8.00	8.10	Mold Flatness		ccc	---	0.10	---
Ball Pitch	X	eD	---	1.00BSC	---	Coplanarity		ddd	---	0.10	---
	Y	eE	---	1.00BSC	---	Ball offset(Package)		eee	---	0.15	---
Mold Thickness		A2	0.51	0.53	0.54	Ball offset(Ball)		fff	---	0.08	---
Substrate Thickness		A3	0.22	0.26	0.30	Edge Ball Center to Center	X	D1	---	3.00BSC	---
Substrate+Mold Thickness+Mold Gap		A4	0.73	0.79	0.84		Y	E1	---	5.00BSC	---
Total Thickness		A	---	---	1.20	Edge Ball Center to Package Edge	X	D2	1.40	1.50	1.60
Ball Diameter			---	0.40	---		Y	E2	1.40	1.50	1.60
Ball Stand Off		A1	---	0.30	---	Ball Center to Body Center	X	SD	---	0.50BSC	---
Ball Width		Øb	0.35	0.40	0.45		Y	SE	---	0.50BSC	---