27011
PAGE-ADDRESSED 1M (8 x 16K x 8) UV ERASABLE PROM

- **Paged Organization**
  - **Reduced Physical Address Requirement**
- **Compatible with 28-Pin JEDEC EPROMs**
  - **Single-Trace Modification for Retrofitting 27128-Based Designs**
- **No-Hardware-Change Upgrades**
  - **Drop-In 27513 Replacement**
- **Fast Programming**
  - **Quick-Pulse Programming™ Algorithm**
  - **Programming Time as Fast as 15 Seconds**
- **Automatic Page Clear**
  - **Resets to Page 0 on Power-Up and On Demand with $\overline{RST}$ Signal(1)**
- **High-Performance HMOS* II-E**
  - **200 ns Access Time**
  - **Low 150 mA Active Power**
- **Standard EPROM Features**
  - **TTL Compatibility**
  - **Two Line Control**
  - **int$_e$ligent Identifier™ for Automated Programming**
- **Smallest Megabit DIP Package**
  - **28-Pin DIP, Minimal Footprint without Address/Data Multiplexing**

The Intel 27011 is a 5V-only, 1,048,576-bit Erasable Programmable Read Only Memory. It is organized as 8 pages of 16K 8-bit words. Its pin-compatibility with byte-wide JEDEC EPROMs allows retrofitting existing designs to the greater storage capacity afforded by the page-addressed organization. Its 16 K-byte physical address space requirement allows the 27011 to be utilized in address-constrained system designs.

When a 28-pin DIP socket is configured for 2764 or 27128 EPROMs, it is easily retrofitted to the 27011. By adding a WRITE ENABLE signal to pin 27 (DIP) or pin 31 (PLCC) (unused on 2764 and 27128), the 27011 can be used in an existing design. Thus, the 27011 enables product enhancements via additional feature sets and firmware-intensive performance upgrades.

The page-addressed organization allows the use of 28-pin DIP packages, the smallest megabit EPROM footprint with applicability to all microprocessors. This provides very efficient circuit board layouts.

The 27011 has an automatic page clear circuit for ease of use of its paged organization. The page-select latch is automatically cleared to the lowest order page upon system power-up. The 27011 also contains many industry-standard features such as two-line output control for simple interfacing and the int$_e$ligent Identifier™ feature for automated programming. It also can be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm.

The 27011 is manufactured using an advanced version of Intel's HMOS* II-E process which assures highest reliability and manufacturability.

*HMOS is a patented process of Intel Corporation.

NOTE:

1. $\overline{RST}$ feature available on all devices shipped from Intel in 1989 and those shipped in 1988 with its 7-digit backside date code beginning with the number '7'.

October 1989
Order Number: 290107-006

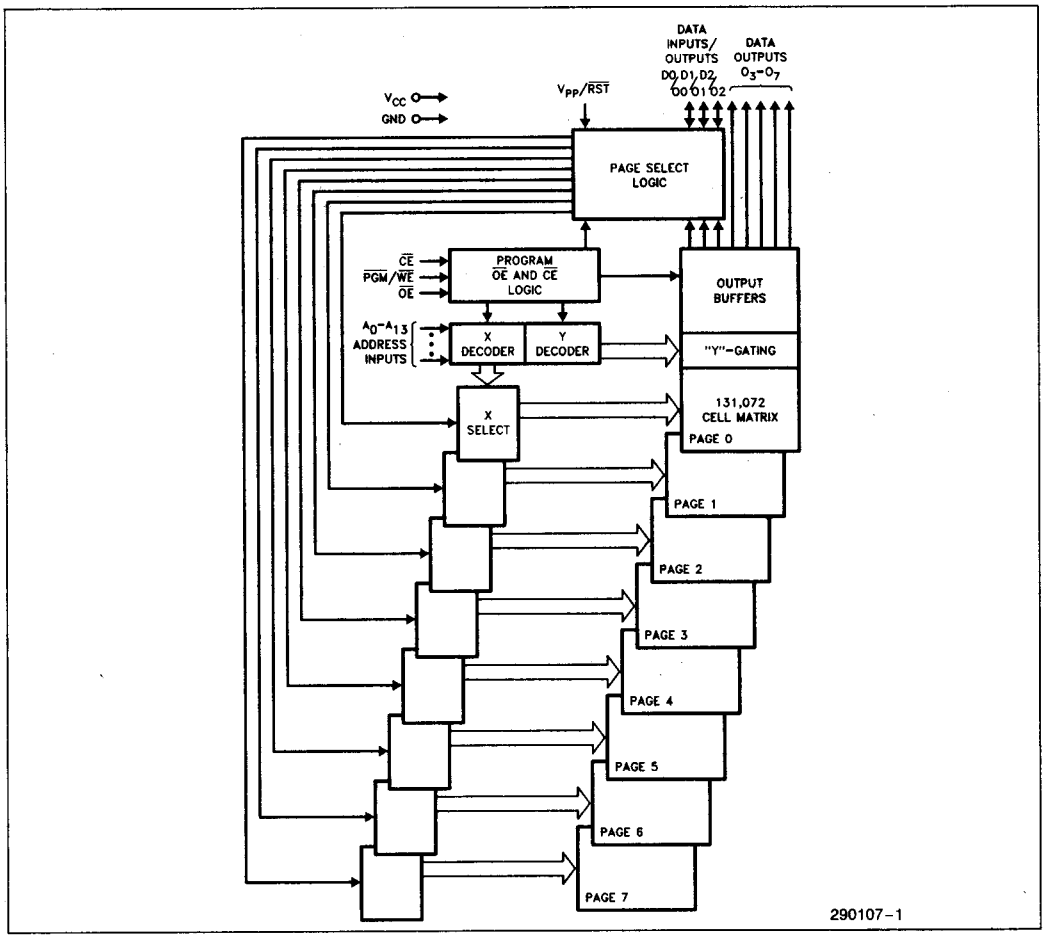
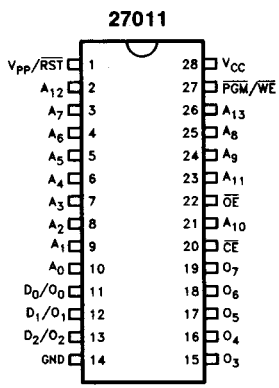


Figure 1. Block Diagram

27513 27C513	27128A 27C128	2764A 27C64 87C64
$\overline{RST}$	V_{PP}	V_{PP}
A_{12}	A_{12}	A_{12}
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0
D_0/O_0	O_0	O_0
D_1/O_1	O_1	O_1
O_2	O_2	O_2
GND	GND	GND



2764A 27C64 87C64	27128A 27C128	27513 27C513
V_{CC} / $\overline{PGM}$	V_{CC} / $\overline{PGM}$	V_{CC} / $\overline{WE}$
N.C.	A_{13}	A_{13}
A_8	A_8	A_8
A_9	A_9	A_9
A_{11} / $\overline{OE}$	A_{11} / $\overline{OE}$	A_{11} / $\overline{OE}/V_{PP}$
A_{10} / $\overline{CE}$	A_{10} / $\overline{CE}$	A_{10} / $\overline{CE}$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

Figure 2. Pin Configuration

Pin Names

A_0–A_{13}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Page-Select Write Enable
O_3–O_7	Outputs
D_X/O_X	Input/Outputs (X = 0, 1, or 2)
$V_{PP}/\overline{RST}$	V_{PP}/Page Reset
N.C.	No Internal Connection
D.U.	Don't Use

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

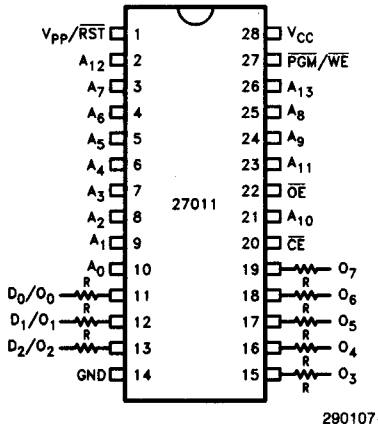
PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

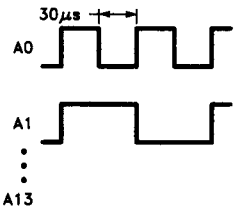
27011 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-250V05	Q, T, L



290107-4

V_{PP} = +5V R = 1 KΩ V_{CC} = +5V
GND = 0V $\overline{CE}$ = GND



290107-5

Binary Sequence from A_0 to A_{13} required for each page. Page changes during burn-in require the following minimum timing parameter values (see Page-Select A.C. Characteristics):

t_{WH} = 500 ns
t_{WP} = 500 ns
t_{WR} = 500 ns
t_{DS} = 500 ns
t_{DH} = 500 ns

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
Read ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with
Respect to Ground† ..... −0.6V to +6.25V
Voltage on A_9 with
Respect to Ground ..... −0.6V to +13.5V
V_{PP} Supply Voltage with Respect to
Ground During Programming .... −0.6V to +14V
V_{CC} Supply Voltage
with Respect to Ground ..... −0.6V to +7.0V

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ(2)	Max		
I_{LI}	Input Load Current			1	µA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	µA	$V_{OUT} = 5.5V$
I_{LRST}(1)	$V_{PP}/\overline{RST}$ Load Current			500	µA	$V_{PP}/\overline{RST} \le V_{CC}$
I_{SB}	V_{CC} Current Standby			50	mA	$\overline{CE} = V_{IH}$
I_{CC1}(4)	V_{CC} Current Active			150	mA	$\overline{CE} = OE = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ µA
V_{CLR}	Page Latch Clear—V_{CC}		3.5	4.0	V	

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Versions	$V_{CC} \pm 5\%$	27011-200V05		27011-250V05		Units
	$V_{CC} \pm 10\%$	27011-200V10		27011-250V10		
Symbol	Characteristics	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		85		100	ns
t_{DF}(3)	$\overline{OE}$ High to Output Float	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		ns

NOTES:
1. $V_{PP}/\overline{RST}$ should be at a TTL V_{IH} level except during programming or during page 0 reset.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

PAGE-SELECT WRITE AND PAGE-RESET OPERATION

A.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

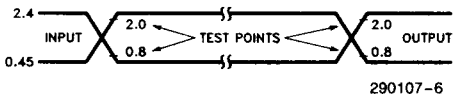
Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
t_{CW}	$\overline{CE}$ to End of Write	180		ns	$\overline{OE} = V_{IH}$
t_{WP}	Write Pulse Width	100		ns	$\overline{OE} = V_{IH}$
t_{WR}	Write Recovery Time	20		ns	
t_{DS}	Data Setup Time	50		ns	$\overline{OE} = V_{IH}$
t_{DH}	Data Hold Time	20		ns	$\overline{OE} = V_{IH}$
t_{CS}	$\overline{CE}$ to Write Setup Time	0		ns	$\overline{OE} = V_{IH}$
t_{WH}	$\overline{WE}$ Low from $\overline{OE}$ High Delay Time	55		ns	
t_{RST}	Reset Low Time	250		ns	
t_{RAV}	Reset to Address Valid	250		ns	

CAPACITANCE(1) $T_A = +25°C$, f = 1 MHz

Symbol	Parameter	Typ(1)	Max	Units	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
$C_{V_{PP}/\overline{RST}}$	$V_{PP}/\overline{RST}$ Capacitance	18	25	pF	$V_{IN} = 0V$

1. Sampled. Not 100% tested.

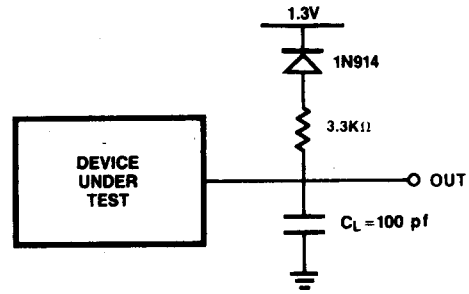
A.C. TESTING INPUT/OUTPUT WAVEFORM



290107-6

AC Testing inputs are driven at 2.4V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at 2.0V for a logic 1 and 0.8V for a logic 0.

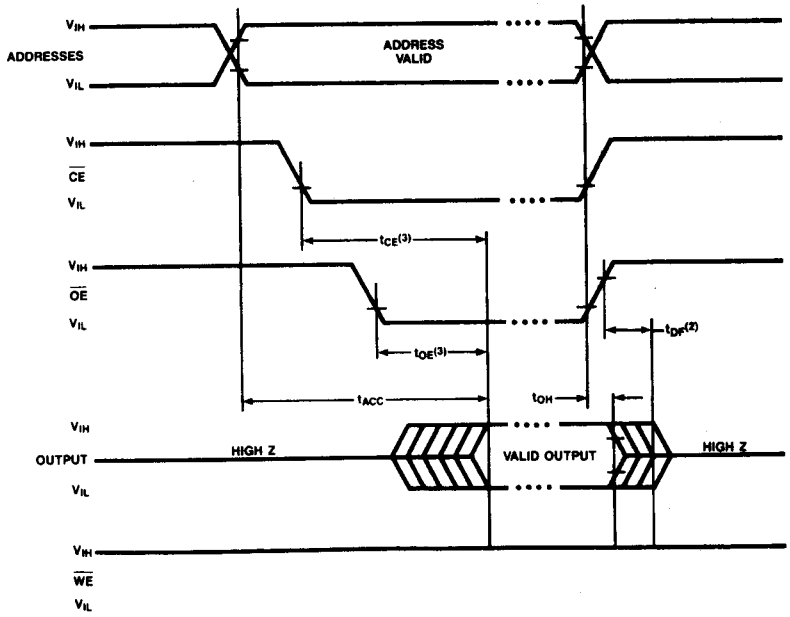
A.C. TESTING LOAD CIRCUIT



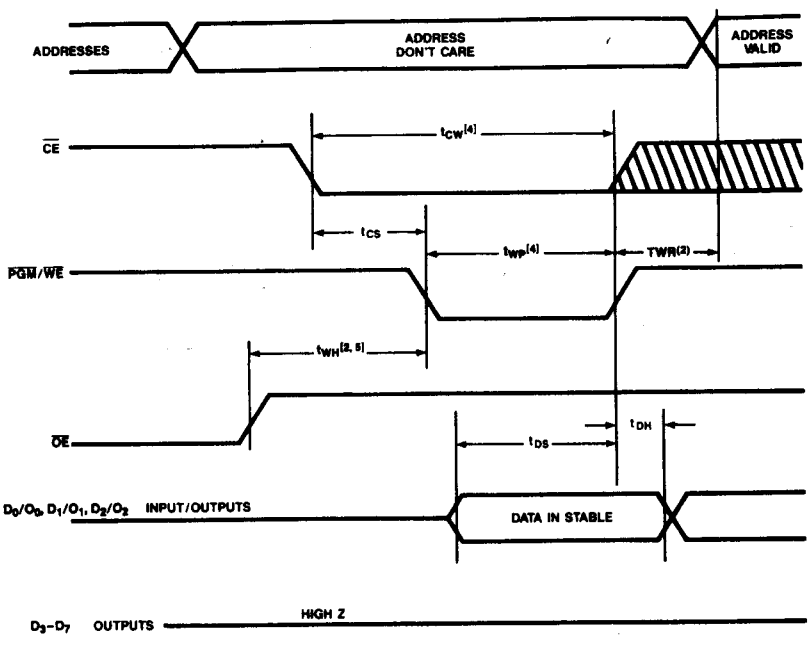
290107-7

C_L = 100 pF
C_L Includes Jig Capacitance

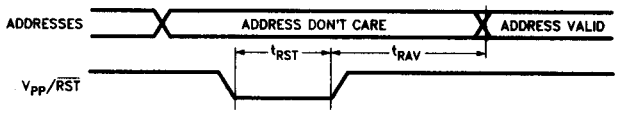
A.C. WAVEFORMS FOR READ OPERATION



A.C. WAVEFORMS FOR PAGE-SELECT WRITE OPERATION



A.C. WAVEFORMS FOR PAGE-RESET OPERATION



NOTES:
1. Typical values are for $T_A = +25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. Write may be terminated by either $\overline{CE}$ or $\overline{WE}$, providing that the minimum t_{CW} requirement is met before bringing $\overline{WE}$ high or that the minimum t_{WP} requirement is met before bringing $\overline{CE}$ high.
5. $\overline{OE}$ must be high during write cycle.

DEVICE OPERATION

The modes of operation of the 27011 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier.

Table 1. Operating Modes

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}/\overline{WE}$	A_9	A_0	$V_{PP}/\overline{RST}$	V_{CC}	Outputs	Input/ Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{IH}	5.0V	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{IH}	5.0V	High Z	High Z
Standby	V_{IH}	X	X	X	X	V_{IH}	5.0V	High Z	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}(3)	V_{CC}(3)	D_{IN}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}(3)	V_{CC}(3)	D_{OUT}	D_{OUT}
Program Inhibit	V_{IH}	X	V_{IH}	X	X	V_{PP}(3)	V_{CC}(3)	High Z	High Z
Page-Select Write	V_{IL}	V_{IH}	V_{IL}	X	X	V_{IH}	V_{CC}(5)	(Note 7)	Page D_{IN}
Page-Reset	X	X	X	X	X	V_{IL}	V_{CC}	(Note 7)	X
int$_e$ligent Identifier —Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(6)	V_{IL}	V_{IH}	5.0V	89H	89H
—Device	V_{IL}	V_{IL}	V_{IH}	V_H(6)	V_{IH}	V_{IH}	5.0V	85H	85H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. Addresses are don't care for page selection. See Table 2 for D_{IN} values.
3. See Table 3 for V_{CC} and V_{PP}.
4. A_1-A_8, $A_{10}-A_{13}$, = V_{IL}.
5. Page 0 is automatically selected at power-up ($V_{CC} < 4.0V$).
6. $V_H = 12.0V \pm 0.5\%$.
7. State of outputs depends on state of $\overline{CE}$ and $\overline{OE}$. See Outputs State for Read, Output Disable, and Standby Modes.

Read Mode

The 27011 has three control functions, two of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. $\overline{WE}$ is held high during read operations.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ and $\overline{WE}$ inputs.

Page-Select Write Mode

The 27011 is addressed by first selecting one of eight 16 K-byte pages. Individual bytes are then selected by normal random access within the 16 K-byte page using the proper combination of A_0–A_{13} address inputs. By applying a TTL low signal to the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high, the desired page is latched in according to the combination of D_0/O_0, D_1/O_1 and D_2/O_2. Address inputs are "don't care" during page selection.

Care should be taken in organizing software programs such that the number of page changes is minimized. This allows maximum system performance. Also, the processor's program counter status must be considered when page changes occur in the middle of an opcode sequence. After a page-select write, the program counter will be incremented to the next location (or further in pipelined systems) in the new page relative to that of the page-select write opcode in the previous page.

Table 2. Page Selection Data

Input/Output / Page Selection	D_2/O_2	D_1/O_1	D_0/O_0
Select Page 0	V_{IL}	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IL}	V_{IH}
Select Page 2	V_{IL}	V_{IH}	V_{IL}
Select Page 3	V_{IL}	V_{IH}	V_{IH}
Select Page 4	V_{IH}	V_{IL}	V_{IL}
Select Page 5	V_{IH}	V_{IL}	V_{IH}
Select Page 6	V_{IH}	V_{IH}	V_{IL}
Select Page 7	V_{IH}	V_{IH}	V_{IH}

Page Reset

The 27011 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latch is automatically cleared to page 0 upon power-up. As the V_{CC} supply voltage ramps up, the page latch is cleared. After V_{CC} exceeds the 4.0V maximum page latch clear voltage (V_{CLR}), the latch clear circuit is disabled. This ensures an adequate safety margin (500 mV of system noise below the worst case -10% V_{CC} supply condition) against spurious page latch clearing.

All 27011 parts shipped in 1989 and those shipped in 1988 with a 7-digit backside date code beginning with the number '7' also have a page reset pin: $V_{PP}/\overline{RST}$. This pin should be tied to an active low reset line. These 27011s will be reset to page 0 when this line is brought to TTL Low (V_{IL}).

Two Line Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 output control lines which accommodate this multiple memory connection. The two control lines for read operation allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Similarly, $\overline{CE}$ deselects other 27011s or RAMs during page select write operation while $\overline{WE}$ is in common with other devices in the array. $\overline{WE}$ is connected to the $\overline{WRITE}$ system control line.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The as-

sociated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be as stable as possible.

PROGRAMMING

Caution: Exceeding 14.0V on V_{PP} will permanently damage the 27011.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 27011 is in the programming mode when the V_{PP} input is at its programming voltage and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 27011s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other 27011s from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27011s may be common. A TTL low-level pulse applied to the $\overline{PGM}/\overline{WE}$ input with V_{PP} at its programming voltage will program the selected 27011.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and V_{CC} is at its programming voltage

Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufcturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

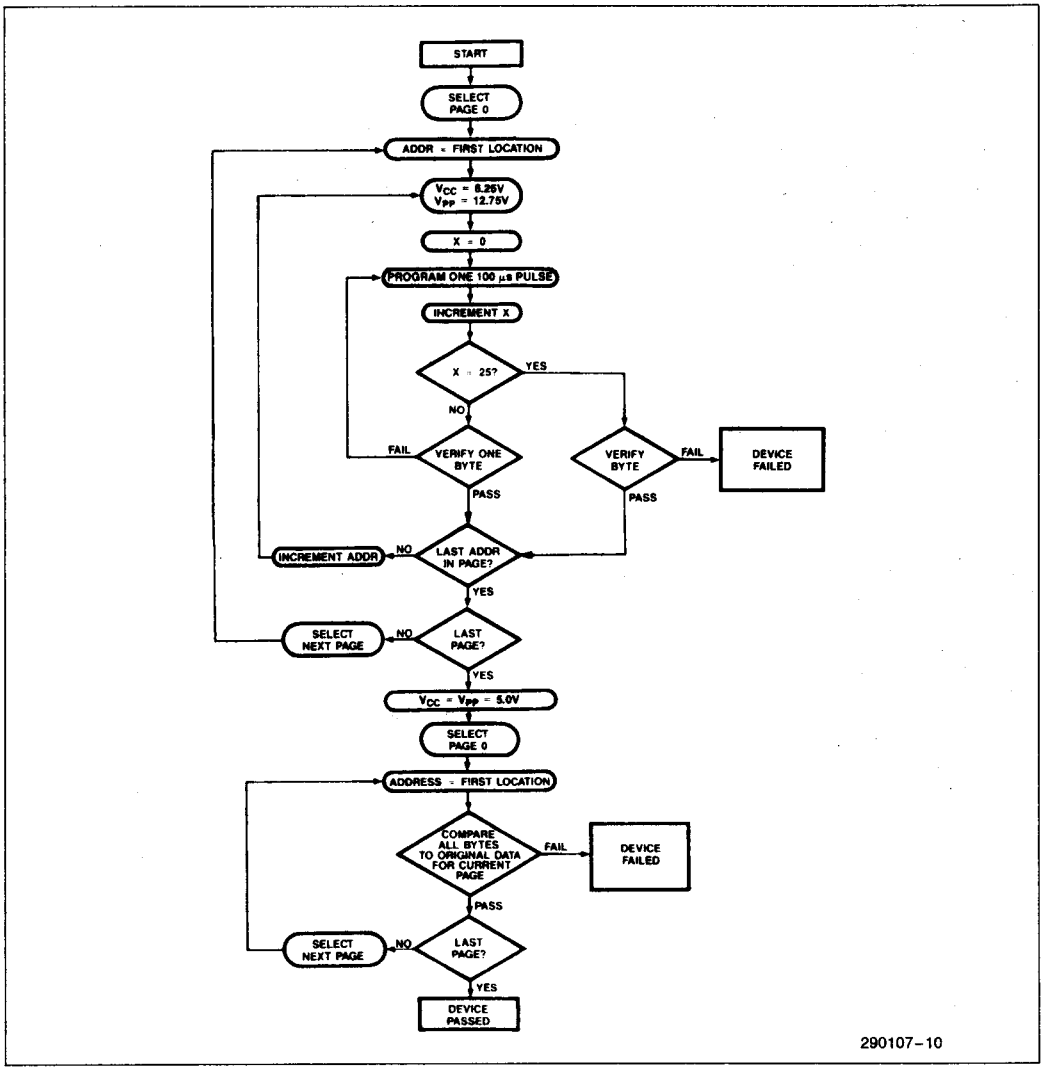


Figure 4. 27011 Quick-Pulse Programming™ Flowchart

Quick Pulse Programming™ Algorithm

Intel's 27011 EPROM is programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows these devices to be programmed as fast as fourteen seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 µs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 4.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP}$ = 5.0V.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 3

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Units	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(3)	V_{CC} Supply Current (Program and Verify)		150	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 3 for V_{CC} and V_{PP} voltages.)

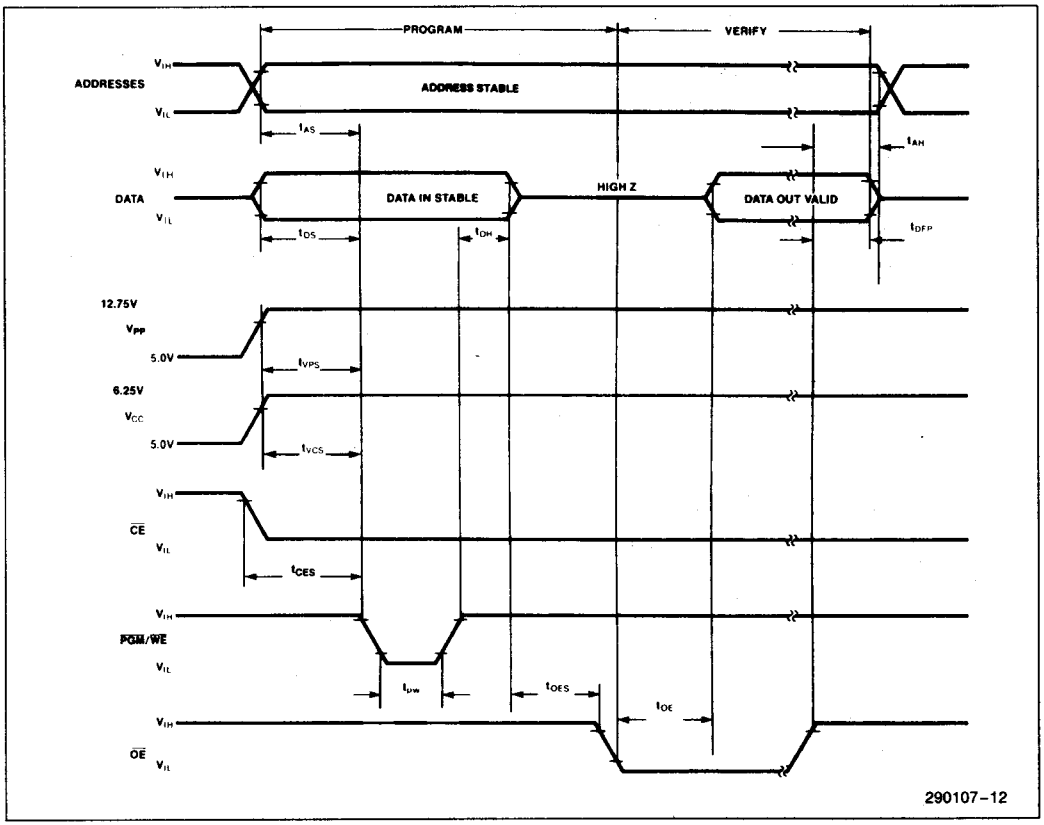
Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Units	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Program Pulse Width	95	100	105	μs	Quick-Pulse Programming
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0–O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for a V_{IL} and 2.0V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page-select write operation prior to programming each of the four 16 Kbyte pages. See Page Select Write AC and DC Characteristics for information on page selection operations.

REVISION HISTORY

Number	Description
06	Revised Express Options Revised Pin Configuration Added **27011-200V10** Speed Bin