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D8748H/D8749H HMOS-E SINGLE-COMPONENT 8-BIT MICROCONTROLLER

- High Performance HMOS-E
- Interval Timer/Event Counter
- Two Single Level Interrupts
- Single 5-Volt Supply
- Over 96 Instructions; 90% Single Byte
- Compatible with 8080/8085 Peripherals
- Easily Expandable Memory and I/O
- Up to 1.35 µs Instruction Cycle; All Instructions 1 or 2 Cycles

The Intel D8749H/D8748H are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS-E process.

The family contains 27 I/O lines, an 8-bit timer/counter, on-chip RAM and on-board oscillator/clock circuits. For systems that require extra capability, the family can be expanded using MCS®-80/MCS®-85 peripherals.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

Device	Internal Memory				
D8749H	2K x 8 EPROM	128 x 8 RAM			
D8748H	1K x 8 EPROM	64 x 8 RAM			



Figure 2. Logic Symbol

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1001	
XTAL 1 🗖 2	39 T1
XTAL 2 🗖 3	38 2 P27
RESET 🗖 4	37 D P26
SS 🗖 s	D8748H 36 DP25
	D8749H 35 P24
EA C 7	34 P17
RD 🗖 8	33 🖬 P16
PSEN C 9	32 115
WR 🗖 10	
ALE 🖸 11	30 P13
080 C 12	29 P12
D81 🗖 13	28 DP11
DB2 C 14	27 D P10
D83 🗖 15	26 🗖 V _{DD}
BD4 C 16	25 PROG
085 C 17	24 P23
	23 D P22
DB ₇ D 19	22 D P21
v _{ss} – 20	21 P20
*SS 220	
	210983-3

Figure 3. Pin Configuration

Table 1. Pin Description (40-Pin DIP)

Symbol	Pin No.	Function
V _{SS}	20	Circuit GND potential.
V _{DD}	26	+ 5V during normal operation.
		Programming power supply (+21V).
V _{CC}	40	Main power supply; + 5V during operation and programming.
PROG	25	Output strobe for 8243 I/O expander.
		Program pulse (+18V) input pin during programming.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P23	21-24	8-bit quasi-bidirectional port. P20–P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
P24-P27 Port 2	35–38	
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the RD, WR strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR.
T0 1 Input pin testable using the conditional transfer instructions. T0 can be designated as a clock output using ENT0 CKL ins		Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CKL instruction.
		Used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
INT	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low) interrupt must remain low for at least 3 machine cycles for proper operation.
RD	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)

Symbol	Pin No.	Function
RESET	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})
		Used during programming.
WR	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
PSEN	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low.)
SS	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction.
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug. (Active high.)
		Used during (18V) programming.
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL $V_{\mbox{\scriptsize IH}}$.)
XTAL2	3	Other side of crystal input.

Table 1. Pin Description (40-Pin DIP) (Continued)

Mnemonic	Description	Bytes	Cycles	Mnemonic	Desc
ACCUMULATOR				ACCUMULATOR	•
ADD A, R	Add register to A	1	1	INC A	Increr
ADD A,@R	Add data	1	1	DEC A	Decre
	memory to A		1	CLR A	Clear
ADD A, #data	Add immediate	2	2	CPL A	Comp
	to A			DAA	Decin
ADDC A, R	Add register with	1	1	SWAP A	Swap
	carry				Α
ADDC A, @R	Add data	1	1	RLA	Rotat
	memory with			RLC A	Rotat
	carry				throu
ADDC A. #data	Add immediate	2	2	RR A	Rotat
//000//, « data	with carry	-	-	RRCA	Rotat
ANL A. R	And register to A	1	1		throu
ANL A, @R	And data	1	1		
	memory to A	'	'		
ANII A # data	And immediate	2	2	IN A, P	Input
ANL A, #data		2	2	OUTL P. A	Outpu
	to A			ANL P, #data	And i
ORL A, R	Or register to A	1	1		to poi
ORL A, @R	Or data memory	1	1	ORL P, #data	Orim
	to A	_		Grier, # data	port
ORLA, #data	Or immediate to	2	2	INS A. BUS	Input
	Α			OUTL BUS, A	Outp
XRL A, R	Exclusive or	1	1	ANL BUS, #data	And i
	register to A			AINL BUS, # data	
XRL A, @R	Exclusive or	1	1		to BU
	data memory to			ORL BUS, #data	Or im
	A				BUS
XRL A, #data	Exclusive or	2	2	MOVD A, P	Input
	immediate to A	_			port t

Table 2. Instruction Set

Mnemonic	Description	Bytes	Cycles
ACCUMULATOR (Continued)		
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RLA	Rotate A left	1	1
RLC A	Rotate A left	1	1
	through carry		
RR A	Rotate A right	1	1
RRC A	Rotate A right	1	1
	through carry		
INPUT/OUTPUT			
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, #data	And immediate	2	2
	to port		
ORL P, #data	Or immediate to	2	2
	port		
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, #data	And immediate to BUS	2	2
ORL BUS, #data	Or immediate to BUS	2	2
MOVD A, P	Input expander port to A	1	2

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Table 2. Instruction Set (Continued)

Mnemonic	Description	Bytes	Cycles
INPUT/OUTPU	T (Continued)	•	•
MOVD P, A	Output A to	1	2
ANLD P. A	expander port		
ANLUP, A	And A to expander	1	2
ORLD P, A	Or A to expander	1	2
	port		
REGISTERS			
INC R	Increment register	1	1
INC @R	Increment data	1	1
	memory	•	•
DEC R	Decrement register	1	1
BRANCH	•		
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register	2	2
,	and skip	-	Ľ
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on $T0 = 0$	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on $T1 = 0$	2	2
JF0 addr	Jump on $F0 = 1$	2	2
JF1 addr	Jump on $F1 = 1$	2	2
JTF addr	Jump on timer flag	2	2
JNI addr	Jump on INT = 0	2	2
JBb addr	Jump on	2	2
	accumulator bit		
SUBROUTINE			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore	1	2
	status		2
FLAGS			
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	Clear flag 0	<u>1</u>	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1
DATA MOVES			
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory	1	1
	to A		. .
MOV A, #data	Move immediate	2	2
	to A		

DATA MOVES (Continued)MOV R, AMove A to register11MOV @R, AMove A to data11memoryMOV R, # dataMove immediate to22MOV @R, # dataMove immediate to22data memoryMOV PSW, AMove PSW to A11MOV PSW, AMove A to PSW11MOV PSW, AMove A to PSW11XCH A, @RExchange A and11registerTCHD A, @RExchange nibble11MOVX A, @RMove external12data memorydata memory to A12MOVP A, @AMove A to external12data memorydata memory12MOVP A, @AMove to A from12movP A, @AMove to A from12MOVP A, @AMove to A from12mov A, TRead11mer/counter11MOV T, ALoad11MOV T, ALoad11STRT TStart timer11STRT TStart counter11STRT TStart timer/11InterruptInterrupt11DIS TONTIDisable external11DIS IDisable external11interruptSelect memory11SEL RB1Select memory11bank 0 <t< th=""><th>Mnemonic</th><th>Description</th><th>Bytes</th><th>Cycles</th></t<>	Mnemonic	Description	Bytes	Cycles
MOV @R, AMove A to data1memoryMOV R, # dataMove immediate to22mOV @R, # dataMove immediate to22data memoryMOV A, PSWMove PSW to A11MOV PSW, AMove A to PSW11MOV PSW, AMove A to PSW11XCH A, RExchange A and11registerregister11XCH A, @RExchange A and11MOVX A, @RMove external12data memoryAA2MOVX A, @RMove to external12data memory to AMOVP A, @RMove to A from1MOVP A, @AMove to A from12movP A, @AMove to A from12MOVP A, @AMove to A from12mov T, ALoad11mer/counter11MOV T, ALoad11STRT CNTStart timer11STRT CNTStart counter11STOP TCNTStop timer/counter11DIS TCNTIDisable external11DIS TCNTIDisable external11SEL RB0Select register11SEL RB1Select memory11Dank 0Select memory11SEL MB1Select memory11Dank 1Select memory11SEL MB1<	DATA MOVES (C			
MOV R, # datamemory Move immediate to register22MOV @R, # dataMove immediate to data memory data memory22MOV A, PSWMove PSW to A11MOV PSW, AMove A to PSW11XCH A, RExchange A and Exchange A and data memory11XCH A, @RExchange A and exchange nibble of A and register11MOVX A, @RMove external data memory to A22MOVX @R, AMove a to external data memory to A22MOVP A, @RMove to A from page 322TIMER/COUNTERImmer/counter mov A, T11MOV T, ALoad timer/counter11STRT TStart timer start counter11STRT TStart timer/ counter11STRT TStart timer/ counter11DIS TCNTIDisable external interrupt11DIS TCNTIDisable external bank 011SEL RB1Select register bank 111SEL RB1Select memory bank 111SEL MB1Select memory bank 111ENTO CLKEnable clock clock11ENTO CLKEnable clock clock11			•	1
MOV R, #dataMove immediate to register22MOV @R, #dataMove immediate to data memory22MOV A, PSWMove PSW to A11MOV PSW, AMove PSW to A11MOV PSW, AMove PSW to A11MOV PSW, AMove PSW to A11XCH A, RExchange A and Exchange nibble11XCH D, @RExchange A and exchange nibble11MOVX A, @RMove external data memory22MOVX A, @RMove external data memory22MOVP A, @AMove to A from page 312TIMER/COUNTERImmer/counter11MOV A, TRead page 311TIMER/COUNTERImmer/counter11MOV T, ALoad timer/counter11STRT TStart timer counter11STRT TStart counter to counter11STRT TStart counter to counter interrupt11DIS TCNTIDisable timer/ to counter interrupt11DIS IDisable external to ank 011SEL RB1Select register bank 111SEL MB1Select memory bank 011SEL MB1Select memory bank 111Enable clock output on T011	MOV @R, A		1	1
registerMOV @R, #dataMove immediate to data memory22MOV A, PSWMove PSW to A11MOV PSW, AMove PSW to A11MOV PSW, AMove A to PSW11XCH A, RExchange A and Exchange A and of A and register11XCH D, @RExchange A and esternal of A and register11MOVX A, @RMove external data memory22MOVX @R, AMove external data memory12MOVP A, @AMove to A from page 322TIMER/COUNTERImmer/counter11MOV T, ALoad timer/counter11STRT TStart timer start timer11STRT TStart counter11STRT TStart timer timer/counter11DIS TCNTIDisable timer/ counter interrupt11DIS TCNTIDisable external interrupt11DIS TCNTIDisable external bank 011SEL RB1Select register bank 011SEL MB1Select memory bank 111SEL MB1Select memory bank 111ENT0 CLKEnable clock cok bank 111				
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of A and register MOVX A, @R Move external 1 2 data memory to A MOVX @R, A Move A to external 1 2 data memory data memory 1 2 MOVP A, @A Move to A from 1 2 MOVP A, @A Move to A from 1 2 move to A from 1 2 2 MOVP A, @A Move to A from 1 2 move to A from 1 2 2 move to A from 1 2 2 MOVA, T Read 1 1 more/counter 1 1 1 MOV T, A Load 1 1 STRT T Start counter 1 1 STOP TCNT Start counter 1 1 STOP TCNT Stapte timer/counter 1 1 DIS TCNTI Disable timer/ 1 1 counter interrupt 1 1 1 DIS TCNTI Disable external 1 1 DIS I <td< td=""><td></td><td></td><td></td><td>4</td></td<>				4
MOVX A, @R Move external data memory to A 1 2 MOVX @R, A Move A to external data memory 1 2 MOVP A, @A Move to A trom 1 2 MOVP A, @A Move to A from 1 2 MOVP A, @A Move to A from 1 2 MOVP A, @A Move to A from 1 2 MOVP A, @A Move to A from 1 2 move to A from 1 2 2 MOV A, T Read 1 1 mer/counter 1 1 1 MOV T, A Load 1 1 STRT Start counter 1 1 STOP TCNT Start counter 1 1 STOP TCNT Stop timer/counter 1 1 DIS TCNTI Disable timer/ 1 1 counter interrupt 1 1 1 DIS TCNTI Disable external 1 1 interrupt 1 1 1 1 DIS I Disable external 1 1 <td></td> <td></td> <td>1</td> <td>1</td>			1	1
data memory to AMOVX @R, AMove A to external12data memory12data memory12MOVP A, @AMove to A from12movP3 A, @AMove to A from11movP3 A, @ALand11movP3 A, @ALand11MOV T, ALoad11STRT TStart timer11STRT CNTStart timer/counter11DIS TCNTIDisable timer/11DIS TCNTIDisable external11DIS IDisable external11DIS IDisable external11SEL RB1Select register11bank 0Select memory11SEL MB1 <td></td> <td></td> <td></td> <td></td>				
MOVX @R, A Move A to external 1 2 data memory MOVP A, @A Move to A from 1 2 MOVP A, @A Move to A from 1 2 move to A from 1 2 2 MOVP3 A, @A Move to A from 1 2 move to A from 1 2 2 move to A from 1 1 1 move to A from 1 1 1 move to A from 1 1 1 for the fract timer 1 1 STRT CNT Start timer 1 1 STOP TCNT Stop timer/counter 1 1 DIS TCNTI Disable timer/ 1 1 counter interrupt 1 1 1 DIS I Disable external 1 1			1	2
data memoryLMOVP A, @AMove to A from12current pageMove to A from12MOVP3 A, @AMove to A from12page 3TIMER/COUNTERmemory11MOV A, TRead111timer/counter111MOV T, ALoad11STRT TStart timer11STRT CNTStart counter11STOP TCNTStop timer/counter11EN TCNTIEnable timer/11DIS TCNTIDisable timer/11DIS TCNTIDisable external11DIS TCNTIDisable external11DIS IDisable external11DIS ISelect register11bank 0Select register11SEL RB0Select memory11bank 1Select memory11SEL MB1Select memory11bank 1Select memory11ENT0 CLKEnable clock11				
MOVP A, @AMove to A from current page12MOVP3 A, @AMove to A from page 312TIMER/COUNTERMOV A, TRead timer/counter11MOV T, ALoad timer/counter11MOV T, ALoad timer/counter11STRT TStart timer start counter11STRT CNTStart counter 	MOVX @H, A		1	2
MOVP3 A, @Acurrent page Move to A from page 312TIMER/COUNTERMOV A, TRead11timer/counter11MOV T, ALoad11timer/counter11STRT TStart timer11STRT CNTStart counter11STOP TCNTStop timer/counter11EN TCNTIEnable timer/ counter interrupt11DIS TCNTIDisable timer/ counter interrupt11DIS TCNTIDisable external interrupt11DIS IDisable external bank 011SEL RB0Select register bank 111SEL MB0Select memory bank 111SEL MB1Select memory bank 111ENT0 CLKEnable clock cok to T011				
MOVP3 A, @A Move to A from page 3 1 2 TIMER/COUNTER MOV A, T Read 1 1 MOV A, T Read 1 1 1 MOV A, T Read 1 1 1 MOV T, A Load 1 1 1 MOV T, A Load 1 1 1 MOV T, A Load 1 1 1 STRT T Start counter 1 1 1 STRT CNT Start counter 1 1 1 STOP TCNT Stop timer/counter 1 1 1 EN TCNTI Enable timer/ 1 1 1 counter interrupt DIS TCNTI Disable timer/ 1 1 DIS TCNTI Enable external 1 1 1 counter interrupt DIS Disable external 1 1 DIS I Disable external 1 1 1 SEL RB0 Select register 1 1 1 bank 0 SEL MB1 Select mem	MOVP A, @A		1	2
page 3 TIMER/COUNTER MOV A, T Read 1 1 MOV T, A Load 1 1 Immer/counter 1 1 1 MOV T, A Load 1 1 MOV T, A Load 1 1 MOV T, A Load 1 1 STRT Start timer 1 1 STRT CNT Start counter 1 1 STOP TCNT Stop timer/counter 1 1 EN TCNTI Enable timer/ 1 1 CONTROL Enable external 1 1 EN I Enable external 1 1 DIS I Disable external 1 1 Bank 0 Select register 1 1 SEL MB0 Select memory 1 1 Bank 0 Select memory <		current page		
TIMER/COUNTER MOV A, T Read 1 1 timer/counter 1 1 1 MOV T, A Load 1 1 1 MOV T, A Load 1 1 1 STRT T Start timer 1 1 1 STRT CNT Start counter 1 1 1 STOP TCNT Stop timer/counter 1 1 1 EN TCNTI Enable timer/ 1 1 1 CONTROL Enable external 1 1 1 EN I Enable external 1 1 1 interrupt DIS I Disable external 1 1 DIS I Disable external 1 1 1 interrupt SEL RB0 Select register 1 1 1 SEL RB1 Select register 1 1 1 1 bank 0 SEL MB1 Select memory 1 1 1 bank 1 Enable clock 1 1 1 1 <td>MOVP3 A, @A</td> <td>Move to A from</td> <td>1</td> <td>2</td>	MOVP3 A, @A	Move to A from	1	2
MOV A, TRead11timer/counter111MOV T, ALoad11timer/counter11STRT TStart timer11STRT CNTStart counter11STOP TCNTStop timer/counter11EN TCNTIEnable timer/11DIS TCNTIDisable timer/11counter interrupt111DIS TCNTIDisable timer/11DIS TCNTIDisable external11DIS IDisable external11DIS IDisable external11bank 0Select register11SEL RB0Select register11bank 1Select memory11bank 0SEL MB1Select memory11bank 1Select memory11bank 1ENT0 CLKEnable clock11		page 3		
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ENT0 CLK Enable clock 1 1 output on T0		-	1	1
output on T0				
	ENTUGER		1	1
NOP No operation 1 1	NOD			
		No operation	1	1

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias 0°C to +70°C
Storage Temperature65°C to +150°C
Voltage On Any Pin With Respect
to Ground
Power Dissipation 1.0 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

			Limits					
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions	Device	
VIL	Input Low Voltage (All Except RESET, X1, X2)	-0.5		0.8	v		All	
V _{IL1}	Input Low Voltage (RESET, X1, X2)	-0.5		0.6	V		Ali	
VIH	Input High Voltage (All Except XTAL1, XTAL2, RESET	2.0		V _{CC}	V	· ·	All	
V _{IH1}	Input High Voltage (X1, X2, RESET)	3.8		V _{CC}	V		Ali	
V _{OL}	Output Low Voltage (BUS)			0.45	>	$l_{OL} = 2.0 \text{ mA}$	All	
V _{OL1}	Output Low Voltage (RD, WR, PSEN, ALE)			0.45	~	I _{OL} = 1.8 mA	All	
V _{OL2}	Output Low Voltage (PROG)			0.45	V	I _{OL} = 1.0 mA	All	
V _{OL3}	Output Low Voltage (All Other Outputs)			0.45	V	I _{OL} = 1.6 mA	All	
V _{OH}	Output High Voltage (BUS)	2.4			V	I _{OH} = -400 μA	All	
V _{OH1}	Output High Voltage (RD, WR, PSEN, ALE)	2.4			V	l _{OH} = −100 μA	All	
V _{OH2}	Output High Voltage (All Other Outputs)	2.4			V	I _{OH} = -40 μA	Ali	
I _{L1}	Leakage Current (T1, INT)			±10	μΑ	$V_{SS} \le V_{IN} \le V_{CC}$	All	
I _{LI1}	Input Leakage Current (P10-P17, P20-P27, EA, SS)			- 500	μΑ	$V_{\text{SS}} + 0.45 \le V_{\text{IN}} \le V_{\text{CC}}$	All	
I _{LI2}	Input Leakage Current RESET	- 10		-300	μA	$V_{SS} \le V_{IN} \le 3.8V$	All	
ILO	Leakage Current (BUS, T0) (High Impedance State)			±10	μΑ	$V_{SS} \le V_{IN} \le V_{CC}$	All	
IDD + ICC	Total Supply Current*		80	100	mA		8748H	
			95	110	mA		8749H	

DC CHARACTERISTICS $T_A = 0^{\circ}C$ to $+70^{\circ}C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

NOTE:

*I_{CC} + I_{DD} is measured with all outputs disconnected; SS, RESET, and INT equal to V_{CC}; EA equal to V_{SS}.

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AC CHARACTERISTICS $T_A = 0^{\circ}C$ to $+70^{\circ}C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	f(t)	11	MHz		Conditions	
	Farameter	(Note 3)	Min	Max	Unit	(Note 1)	
t	Clock Period	1/xtal freq	90.9	1000	ns	(Note 3)	
t _{LL} ALE Pulse Width		3.5t - 170	150		ns		
t _{AL} Addr Setup to ALE		2t - 110	70		ns	(Note 2)	
t _{LA}	Addr Hold from ALE	t - 40	50		ns		
t _{CC1}	Control Pulse Width (RD, WR)	7.5t - 200	480		ns		
tcc2	Control Pulse Width (PSEN)	6t - 200	350	1	ns		
t _{DW}	Data Setup before WR	6.5t - 200	390	· ····	ns		
twp	Data Hold after WR	t - 50	40		ns		
t _{DR}	Data Hold (RD, PSEN)	1.5t - 30	0	110	ns		
t _{RD1}	RD to Data In	6t - 170		375	ns		
t _{RD2}	PSEN to Data In	4.5t - 170		240	ns		
t _{AW}	Addr Setup to WR	5t - 150	300		ns		
t _{AD1}	Addr Setup to Data (RD)	10.5t - 220		730	ns	·····	
t _{AD2}	Addr Setup to Data (PSEN)	7.5t - 200		460	ns		
tAFC1	Addr Float to RD, WR	2t - 40	140		ns	(Note 2)	
t _{AFC2}	Addr Float to PSEN	0.5t - 40	10		ns	(Note 2)	
t _{LAFC1}	ALE to Control (RD, WR)	3t – 75	200		ns		
tLAFC2	ALE to Control (PSEN)	1.5t - 75	60		ns		
t _{CA1}	Control to ALE (RD, WR, PROG)	t – 65	25		ns		
t _{CA2}	Control to ALE (PSEN)	4t - 70	290		ns		
t _{CP}	Port Control Setup to PROG	1.5t – 80	50		ns	<u> </u>	
t _{PC}	Port Control Hold to PROG	4t – 260	100		ns		
t _{PR}	PROG to P2 Input Valid	8.5t - 120		650	ns		
t _{PF}	Input Data Hold from PROG	1.5t	0	140	ns	·····	
t _{DP}	Output Data Setup	6t – 290	250		ns		
t _{PD}	Output Data Hold	1.5t – 90	40		ns		
tpp	PROG Pulse Width	10.5t - 250	700		ns		
tpL	Port 2 I/O Setup to ALE	4t – 200	160		ns		
t _{LP}	Port 2 I/O Hold to ALE	0.5t - 30	15		ns		
t _{PV}	Port Output from ALE	4.5t + 100		510	ns	<u></u>	
toprr	T0 Rep Rate	3t	270		ns	······	
t _{CY}	Cycle Time	15t	1.36	15.0	μs	-	

NOTES:

1. Control outputs CL = 80 pF; BUS outputs CL = 150 pF.

2. BUS High Impedance Load 20 pF.

3. f(t) assumes 50% duty cycle on X1, X2. Max clock period is for a 1 MHz crystal input.



WAVEFORMS

INSTRUCTION FETCH FROM PROGRAM MEMORY



READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL DATA MEMORY



INPUT AND OUTPUT FOR AC TESTS



D8748H/D8749H

PORT 1/PORT 2 TIMING



CRYSTAL OSCILLATOR MODE



CERAMIC RESONATOR MODE



1



DRIVING FROM EXTERNAL SOURCE



PROGRAMMING, VERIFYING AND ERASING THE 8749H (8748H) EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock Input (3 to 4.0 MHz)
XTAL 2	
RESET	Initialization and Address Latching
TEST 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input
	Data Output During Verify
P20-P22	Address Input
V _{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING

An attempt to program a missocketed 8749H (8748H) will result in severe damage to the part. An indication of a property socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

- 1) $V_{DD} = 5V$, Clock applied or internal oscillator operating. RESET = 0V, TEST 0 = 5V, EA = 5V, BUS and PROG floating. P10 and P11 must be tied to ground.
- 2) Insert 8749H (8748H) in programming socket.
- 3) TEST 0 = 0V (select program mode)
- 4) EA = 18V (activate program mode)
- 5) Address applied to BUS and P20-22
- 6) RESET = 5V (latch address)
- 7) Data applied to BUS
- 8) V_{DD} = 21V (programming power)
- 9) PROG = V_{CC} or float followed by one 50 ms pulse to 18V
- 10) $V_{DD} = 5V$
- 11) TEST 0 = 5V (verify mode)
- 12) Read and verify data on BUS
- 13) TEST 0 = 0V
- 14) RESET = 0V and repeat from step 5
- 15) Programmer should be at conditions of step 1 when 8749H (8748H) is removed from socket.

AC TIMING SPECIFICATION FOR PROGRAMMING 8748H/8749H

 $T_A = 25^{\circ}C \pm 5^{\circ}C; V_{CC} = 5V \pm 5\%; V_{DD} = 21V \pm 0.5V$

Symbol	Parameter	Min	Max	Unit	Test Conditions
t _{AW}	Address Setup Time to RESET ↑	4t _{CY}			
t _{WA}	Address Hold Time after RESET 1	4t _{CY}			
t _{DW}	Data in Setup Time to PROG ↑	4t _{CY}			
t _{WD}	Data in Hold Time after PROG ↓	4t _{CY}			· · · · · · · · · · · · · · · · · · ·
t _{PH}	RESET Hold Time to Verify	4tcy			
t _{VDDW}	V _{DD} Hold Time before PROG 1	0	1.0	ms	
t _{VDDH}	V _{DD} Hold Time after PROG ↓	0	1.0	ms	
tpw	Program Pulse Width	50	60	ms	
t _{TW}	TEST 0 Setup Time for Program Mode	4t _{CY}			
twr	TEST 0 Hold Time after Program Mode	4t _{CY}			<u> </u>
tDO	TEST 0 to Data Out Delay		4t _{CY}		
tww	RESET Pulse Width to Latch Address	4t _{CY}			·······
t _r , t _f	V _{DD} and PROG Rise and Fall Times	0.5	100	μs	
t _{CY}	CPU Operation Cycle Time	3.75	5	μs	
t _{RE}	RESET Setup Time before EA ↑	4t _{CY}			

NOTE:

If TEST 0 is high, t_{DO} can be triggered by RESET \uparrow .

DC SPECIFICATION FOR PROGRAMMING 8748H/8749H

 $T_A = 25^{\circ}C \pm 5^{\circ}C; V_{CC} = 5V \pm 5\%; V_{DD} = 21V \pm 0.5V$

Symbol	Parameter	Min	Max	Unit	Test Conditions
V _{DDH}	V _{DD} Program Voltage High Level	20.5	21.5	V	
V _{DDL}	V _{DD} Voltage Low Level	4.75	5.25	v	
VPH	PROG Program Voltage High Level	17.5	18.5	v	
V _{PL}	PROG Voltage Low Level	4.0	Vcc	v	
VEAH	EA Program or Verify Voltage High Level	17.5	18.5	v	
IDD	V _{DD} High Voltage Supply Current		20.0	mA	
IPROG	PROG High Voltage Supply Current		1.0	mA	
I _{EA}	EA High Voltage Supply Current		1.0	mA	,

int_{el}.

WAVEFORMS

COMBINATION PROGRAM/VERIFY MODE (EPROMs ONLY)



VERIFY MODE



SUGGESTED EPROM VERIFICATION ALGORITHM FOR HMOS-E DEVICE ONLY

